Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering

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ABSTRACT

We have combined the benefits of the fully depleted TriGate transistor architecture with high-k gate dielectrics, metal gate electrodes and strain engineering. High performance NMOS and PMOS trigate transistors are demonstrated with I_{DSAT}=1.4mA/um and 1.1mA/um respectively (I_{OFF}=100nA/um, V_{CC}=1.1V and L_G=40nm) with excellent short channel effects (SCE) – DIBL and subthreshold swing, ΔS. The contributions of strain, the <100> vs. <110> substrate orientations, high-k gate dielectrics, and low channel doping are investigated for a variety of channel dimensions and FIN profiles. We observe no evidence of early parasitic corner transistor turn-on in the current devices which can potentially degrade I_{ON}-I_{OFF} and ΔS.

I. INTRODUCTION

In order to continue scaling according to Moore's Law beyond the 32nm technology node, a number of fully depleted devices have been proposed to deal with SCE degradation including the DST, FINFET, Surround Gate, MBCFET, and TriGate [1-4]. The Trigate transistor architecture introduces the fewest changes to conventional planar transistor processing. In this work the combination of ultra thin high-k gate dielectric, near mid-gap metal gate workfunction, low doping in the channel and optimized FIN dimensions enable us to fully enhance the gate to channel coupling in TriGate devices for much improved short channel effects. We implement aggressively scaled spacers, ultra shallow abrupt junctions, raised source/drains, strain engineering and high aspect ratio silicon FINS to improve R_{EXT}.

II. EXPERIMENT

TriGate FIN patterning is achieved using a reactive ion etching process, optimized to achieve highly vertical sidewall profiles for improved SCE control as discussed in section III. The <100> substrates are notch oriented so as to expose the <110> plane on the two adjacent vertical sidewalls of the Trigate FIN. The FIN height, H_{Si}, and FIN width, W_{Si}, define the total width of the device as $W_T = 2xH_{Si} + W_{Si}$ (Fig. 1). The gate stack is formed by atomic layer deposition (ALD) of a 20A HfO_2 high-k dielectric, followed by PVD metal deposition which sets the workfunction near mid-gap and CVD deposited polysilicon to complete the gate electrode. The highly vertical yet selective gate patterning is achieved by a combination of dry and wet etch chemistries which prevent notching under the gate, gate profile flare, or breakthrough during the significant over-etch required to clear the polysilicon and metal stringers surrounding the FIN. Following tip-extension implant and spacer formation we introduce selective silicon (NMOS) and embedded SiGe (PMOS) epitaxy for raised source/drains. Tensile strained nitride layers patterned over NMOS transistors are also investigated to enhance electron mobility [5].

III. RESULTS & ANALYSIS

The impact of the silicon FIN etch used to define W_{Si} is illustrated in Figs. 1a, 1b & 1c. If the body dimensions taper outwards towards the bottom of the FIN (Fig. 1a) we observe a marked increase in DIBL and ΔS, Figs. 2a & 2b, as a function of L_{eff}/W_{eff}. Here L_{eff} is defined as the physical gate length, L_G, minus twice the tip overlap region while $W_{eff}=W_{Si}+2\{\varepsilon_{Si}/\varepsilon_{OX}\}* T_{OX}$. This increase in SCE's arises from the weaker electrostatic gate coupling by the side gates as W_{Si} widens near the bottom of the FIN. In the extreme case of a notched profile (Fig.1b) SCE continue to improve but at the expense of yield due to polysilicon/metal stringers along the FIN perimeter. In Fig. 3 we illustrate that by careful optimization of the vertical channel dopant profile one can significantly improve SCE's as a function of L_{eff}/W_{eff}. The near mid-gap workfunction allows us to set the V_T of the TriGate devices with a significantly lower dopant concentration ($10^{17}cm^{-3}$) in the channel as compared to the planar bulk Si technology. This in turn enables stronger gate coupling, improved channel mobility and volume inversion to occur. The combination of a) lower doping in the channel, b) the 4nm top corner radius, R_C, and c) ultra-thin T_{OX} from the high-k dielectric/metal gate stack eliminate any early parasitic corner device turn-on [6-8].

Next, we illustrate the impact of the <110> sidewall surface on the carrier mobility as a function of inversion charge density, Q_{INV}. In Figure 4a, only a minimal 8% degradation is observed in the high field electron mobility for the <110> dominated Trigate device compared to planar <100>. In contrast, Fig.4b illustrates a 100% increase in hole mobility for the <110> transport plane compared to a <100> planar device.

For a given FIN width, W_{Si}=25nm, and increasing H_{Si}, Fig. 5 demonstrates the improvement in normalized R_{D-Lin} due to reduced current crowding with increasing FIN cross-sectional area. The increased H_{Si} also leads to a correspondingly larger contact area and hence a lower contact resistance. Current spreading is further facilitated through the use of a raised silicon source/drain epitaxy. Finally, a conformal tensile strained nitride film is applied to enhance electron mobility in the channel. Figure 6 shows a 35% increase in normalized short channel mobility for tensile versus unstrained nitride layers.

For PMOS Trigates we introduce in-situ boron doped SiGe raised source/drains as illustrated in x and y direction cross-sections of Figs. 7a & 7b. This process element improves the contact resistance due to the lower valence band energy level for SiGe, reduces current crowding and enhances the bulk source/drain conductivity. This is illustrated in Figs. 8a & 8b where we observe a 40% increase in I_{DLin} and a corresponding 40% decrease in R_{DSLin} if the SiGe is embedded into the channel region via an undercut etch prior to epi deposition versus the raised source/drain SiGe case without the undercut etch. The larger lattice constant of the SiGe film can potentially also introduce uniaxial compressive strain for improved hole mobility. The resultant Ion-Ioff, I_D-V_G, and I_D-V_D characteristics for NMOS and PMOS Trigate devices are presented in Figs. 9-11 with their extracted SCE characteristics – I_{OFF}, ΔS_{Sat}, ΔS_{Lin} & DIBL.

IV. CONCLUSIONS

Fully depleted Trigate devices with high-k gate dielectrics, mid-gap metal gates, strained channel engineering and epitaxially grown raised source/drains have been successfully demonstrated. Excellent performance is achieved with NMOS and PMOS I_{Dsat} exceeding 1.4mA/μm and 1.1mA/μm respectively and well controlled SCE's. We attribute this to careful optimization of FIN dimensions, tip extensions and channel doping profiles, ultra-thin T_{OX} and by taking advantage of the improved hole mobility on the <110> plane.

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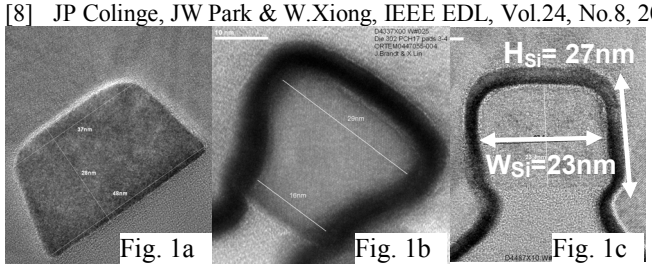

Fig. 1 Various FIN etch profiles illustrating from left to right: 1a) the tapered, 1b) notched and 1c)vertical FIN profiles.

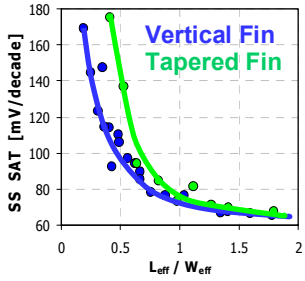

Fig. 2a Subthreshold swing, ΔS_{Sat} for a vertical vs. tapered fin etch

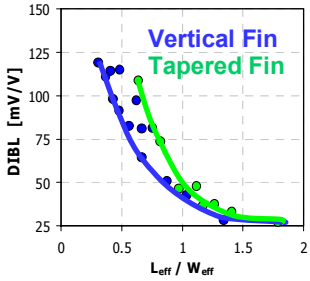

Fig. 2b DIBL comparison for a vertical vs. tapered FIN etch

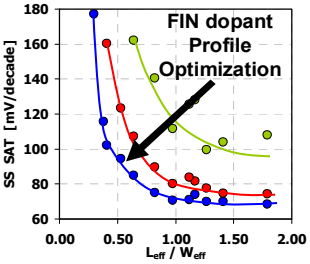

Fig. 3a Subthreshold swing versus various halo doping profiles.

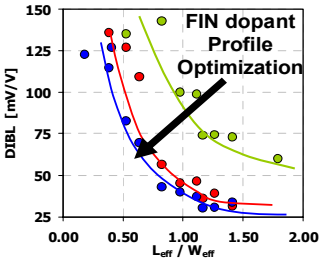

Fig.3b DIBL as a function of the halo doping profile in the channel.

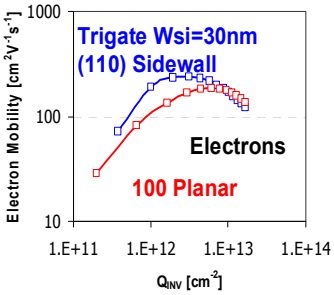

Fig. 4a Electron mobility comparison of a planar <100> vs. a Trigate Trigate <110> dominated device.

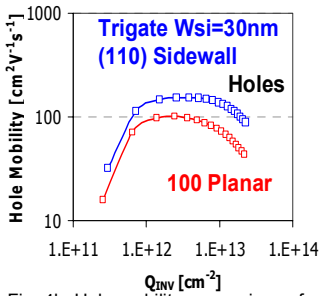

Fig. 4b Hole mobility comparison of a planar <100> vs. a Trigate <110> dominated device.

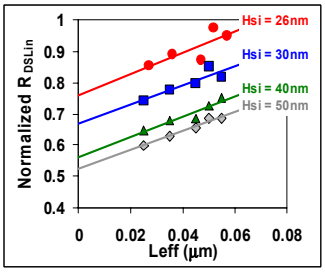

Fig. 5 R_{DSLin} as a function of increasing fin height , H_{Si}.

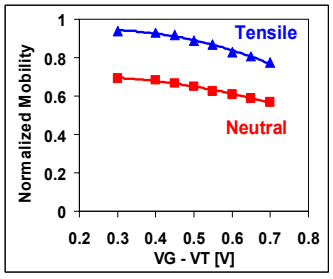

Fig. 6 Normalized electron mobility for tensile versus neutral strain.

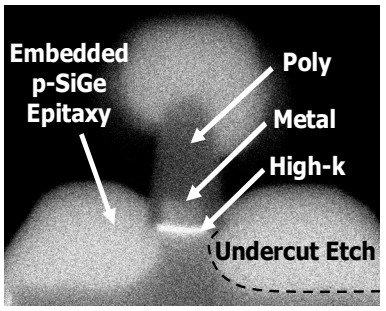

Fig. 7a X-dir. cross-section of PMOS Trigate with SiGe raised source/drains

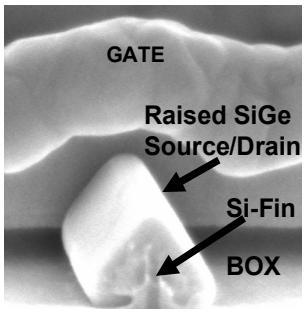

Fig. 7b Y-dir. cross-section of PMOS Trigate with SiGe raised source/drain

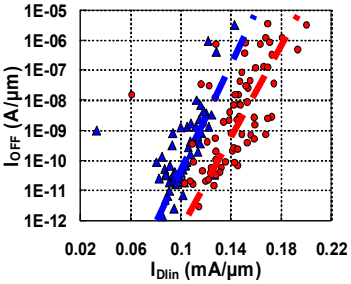

Fig. 8a I_{DLin} versus Ioff for SiGe raised with & without undercut etch.

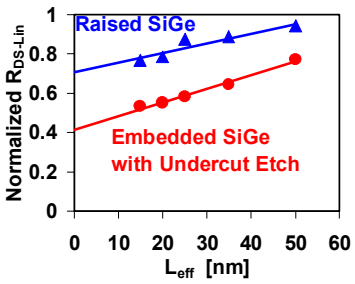

Fig. 8b Normalized R_{DSLin} for SiGe raised epi with & without undercut etch

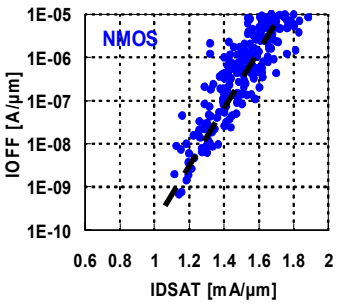

Fig. 9a $I_{ON} - I_{OFF}$ for NMOS Trigate devices at V_{CC}=1.1V

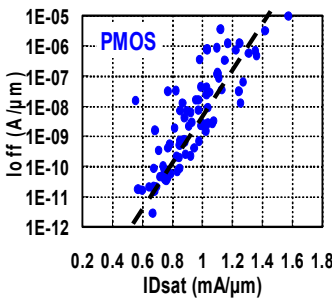

Fig. 9b I_{ON}-I_{OFF} for PMOS Trigate devices at V_{CC}=1.1V

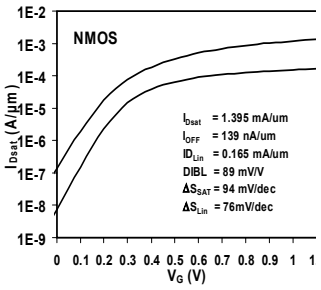

Fig. 10a $I_D - V_G$ for NMOS Trigate device at V_{DS}=1.1V & 0.05V

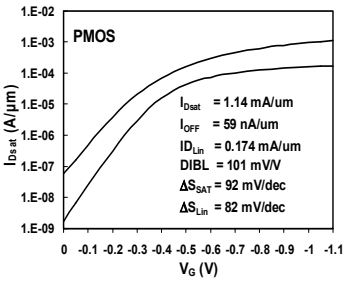

Fig. 10b I_D-V_G for PMOS Trigate device at V_{DS}=1.1 and 0.05V

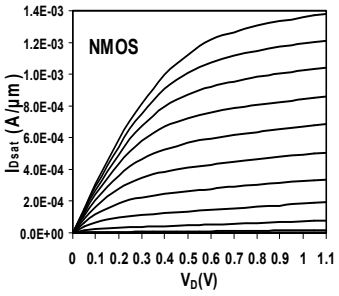

Fig. 11a I_D–V_D family of curves for an NMOS TriGate device.

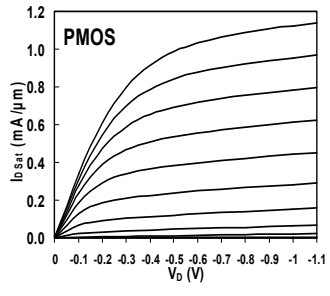

Fig. 11b I_D-V_D family of curves for a PMOS Trigate device.