Intel® Embedded Processor for 2008 (Tolapai) SoC Architecture Overview

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Session ID: QATS001

Intel Developer FORUM

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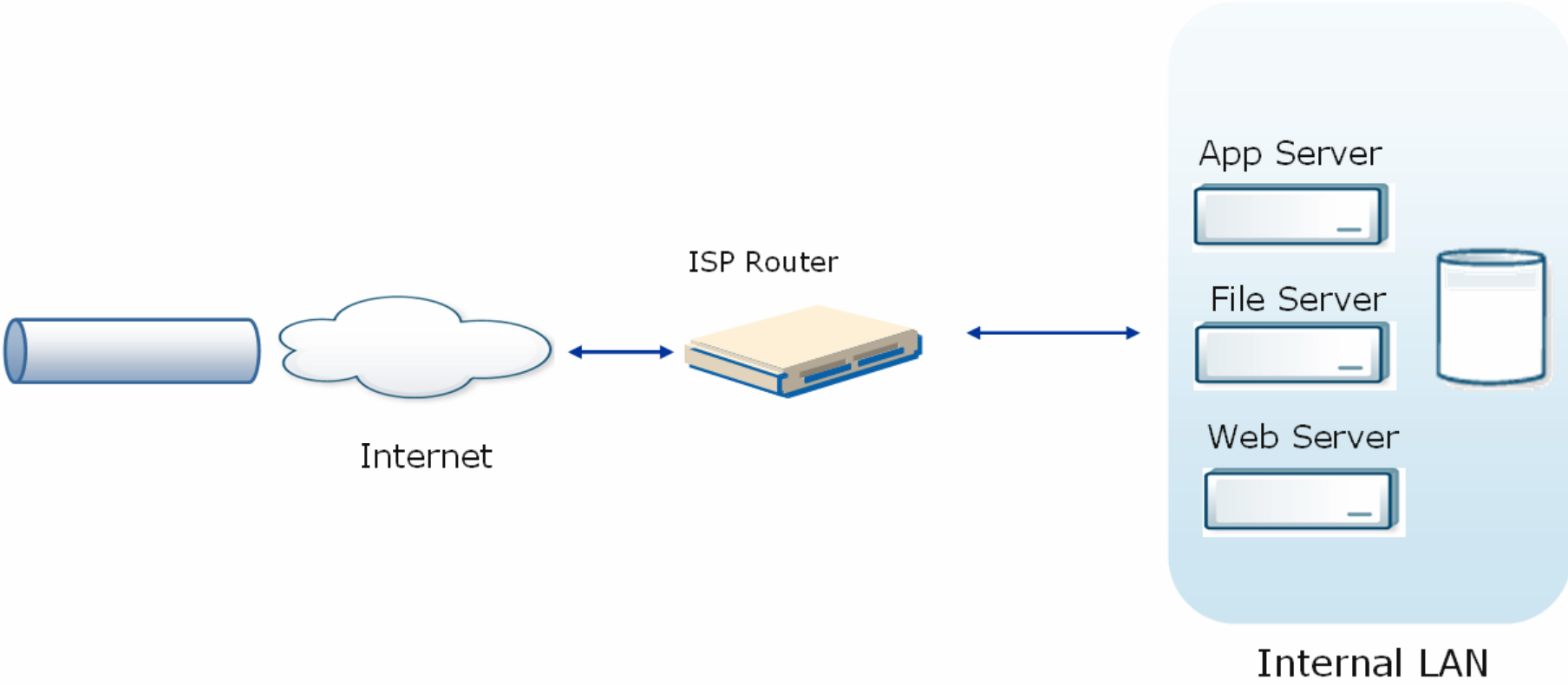
Agenda

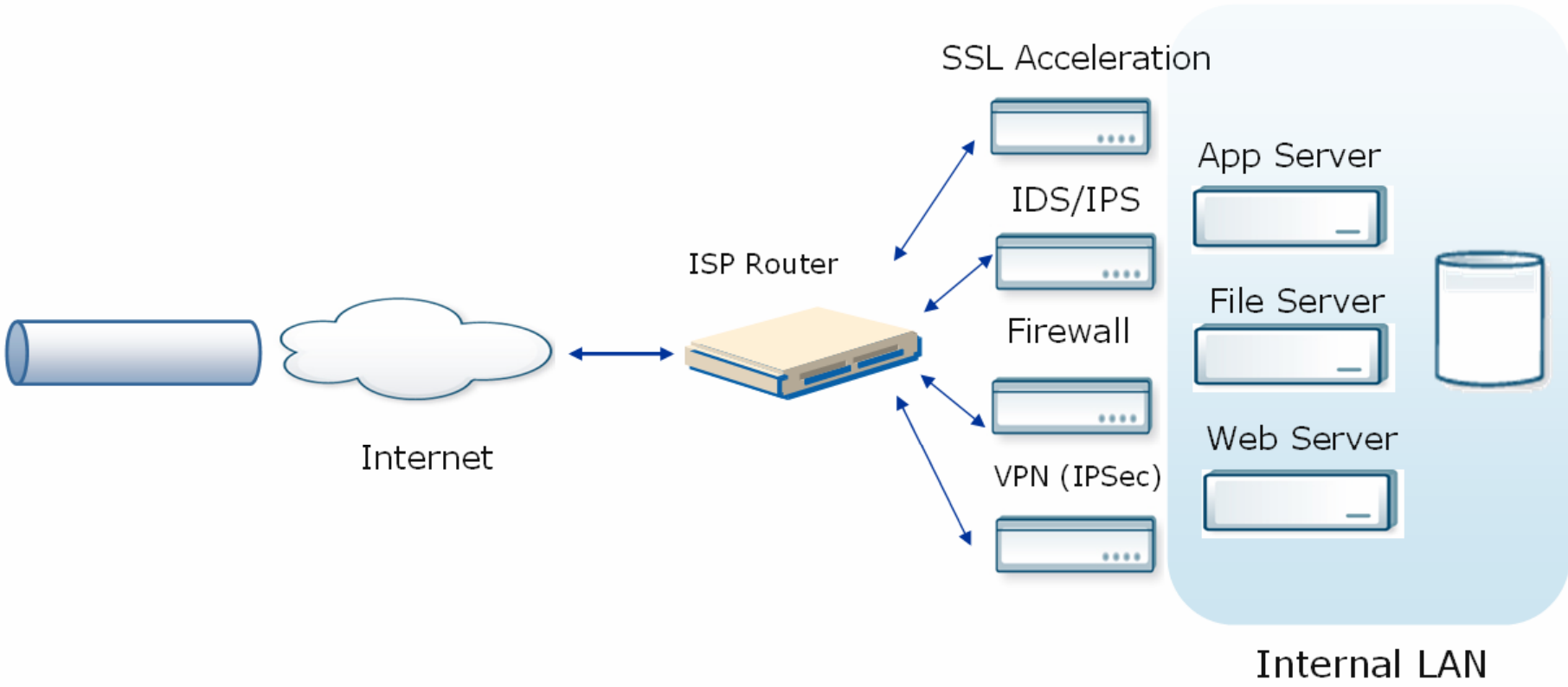
- Usage Needs of Small/Medium Enterprise
- Tolapai Architecture Overview
- Tolapai Silicon Architecture
- Tolapai Software Architecture
- Solving SME Usage Needs

Data Flow within an SME

A Brute Force Approach

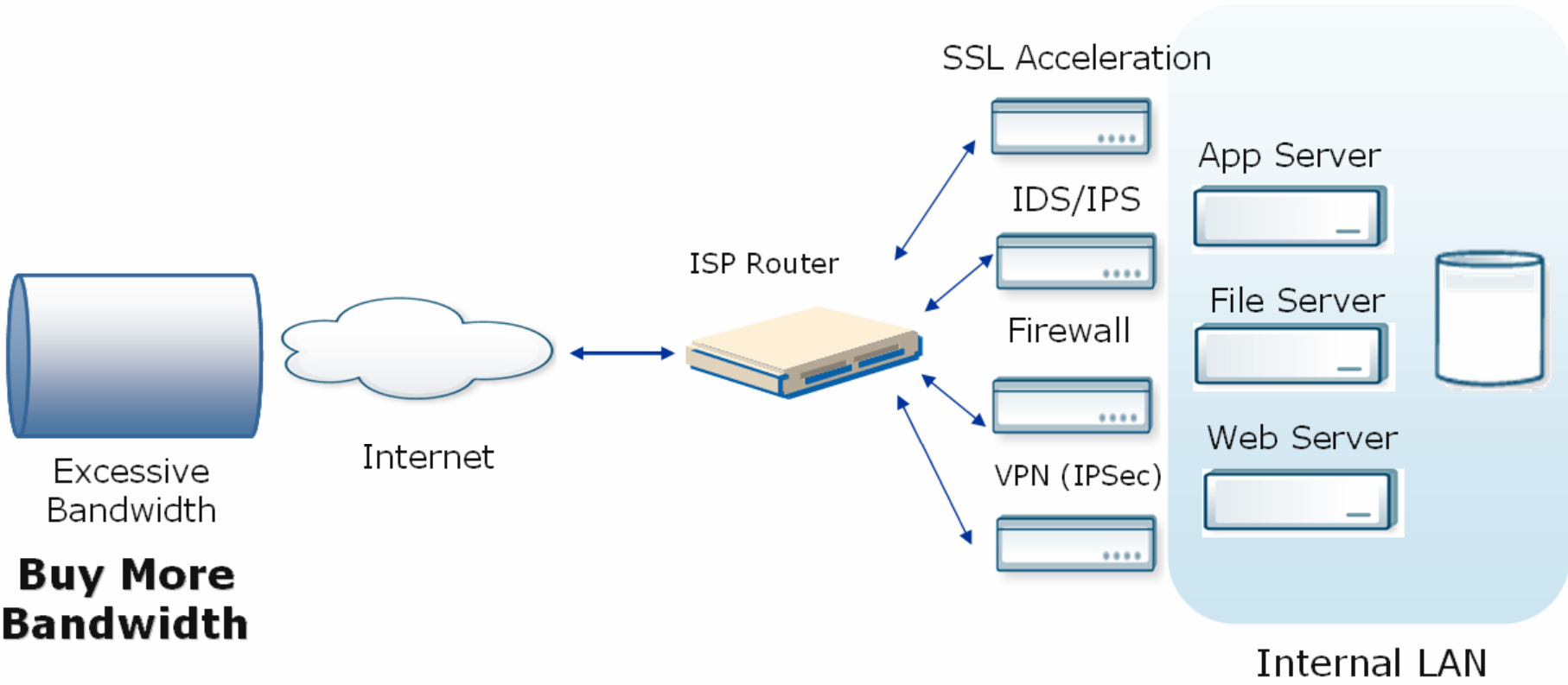


A Brute Force Approach



Buy More Point Products

A Brute Force Approach

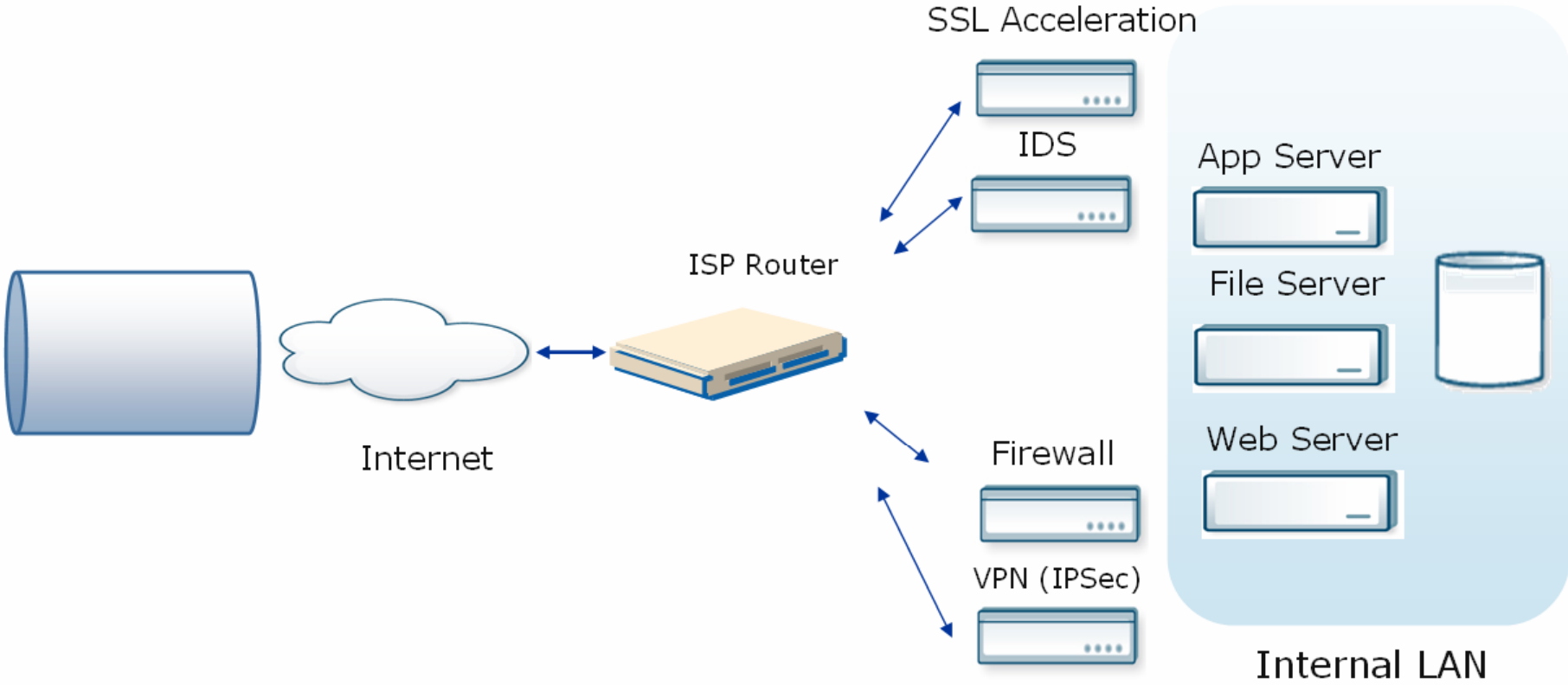


Buy More Bandwidth

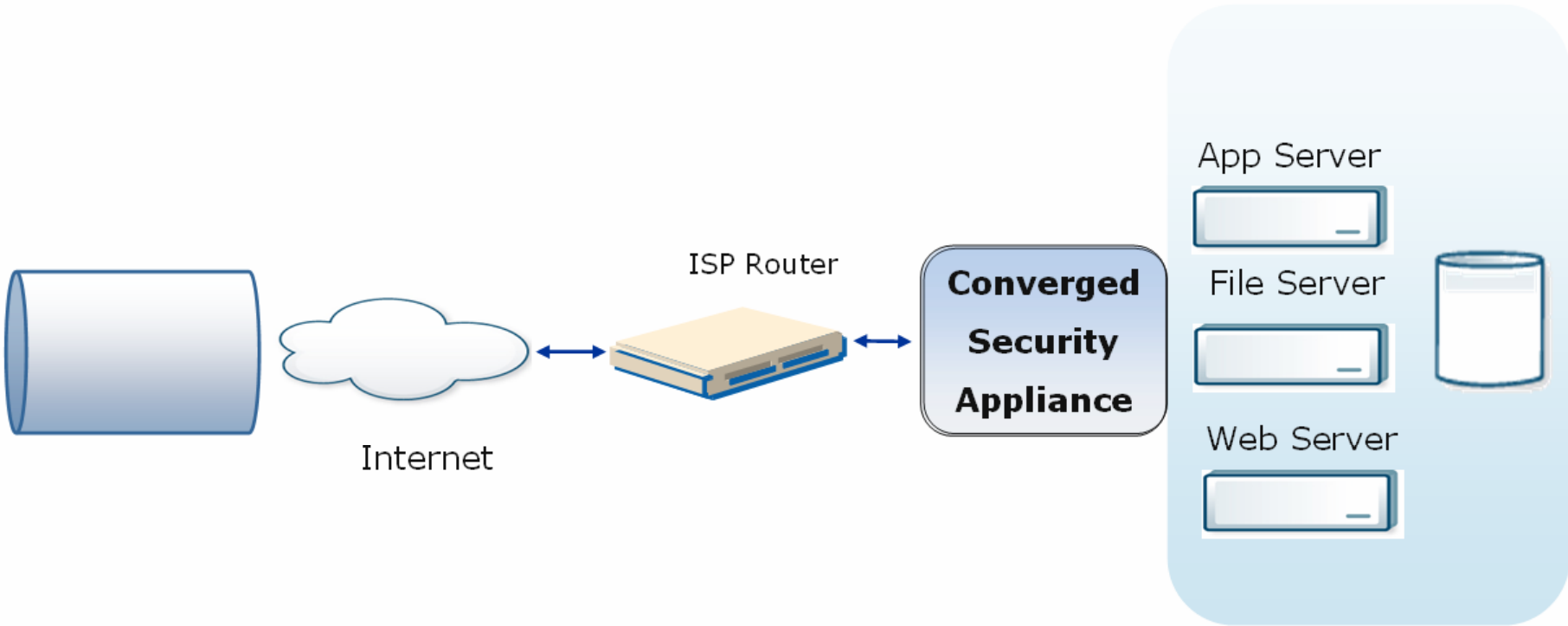
Buy More Point Products

Result: ✓Expensive ✓Complex ✓Slow ✓Doesn't Scale

Emerging SME Solution

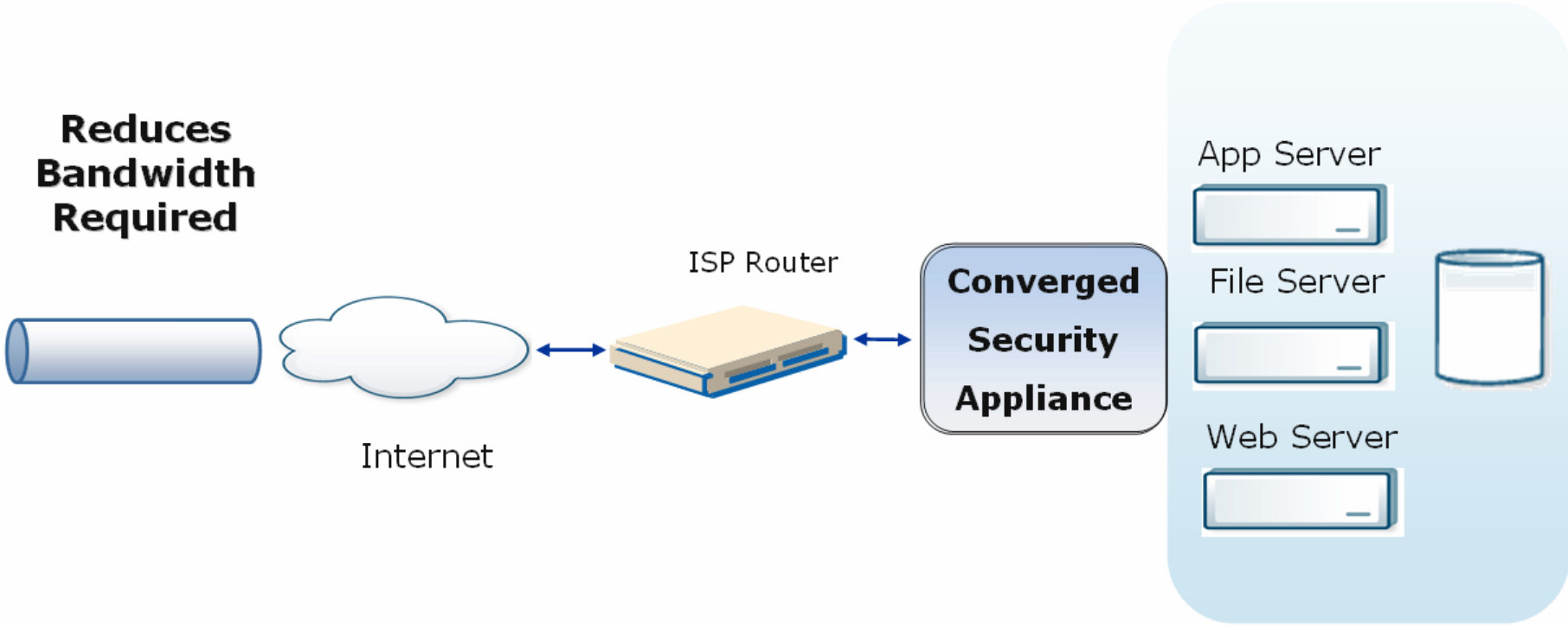


Emerging SME Solution



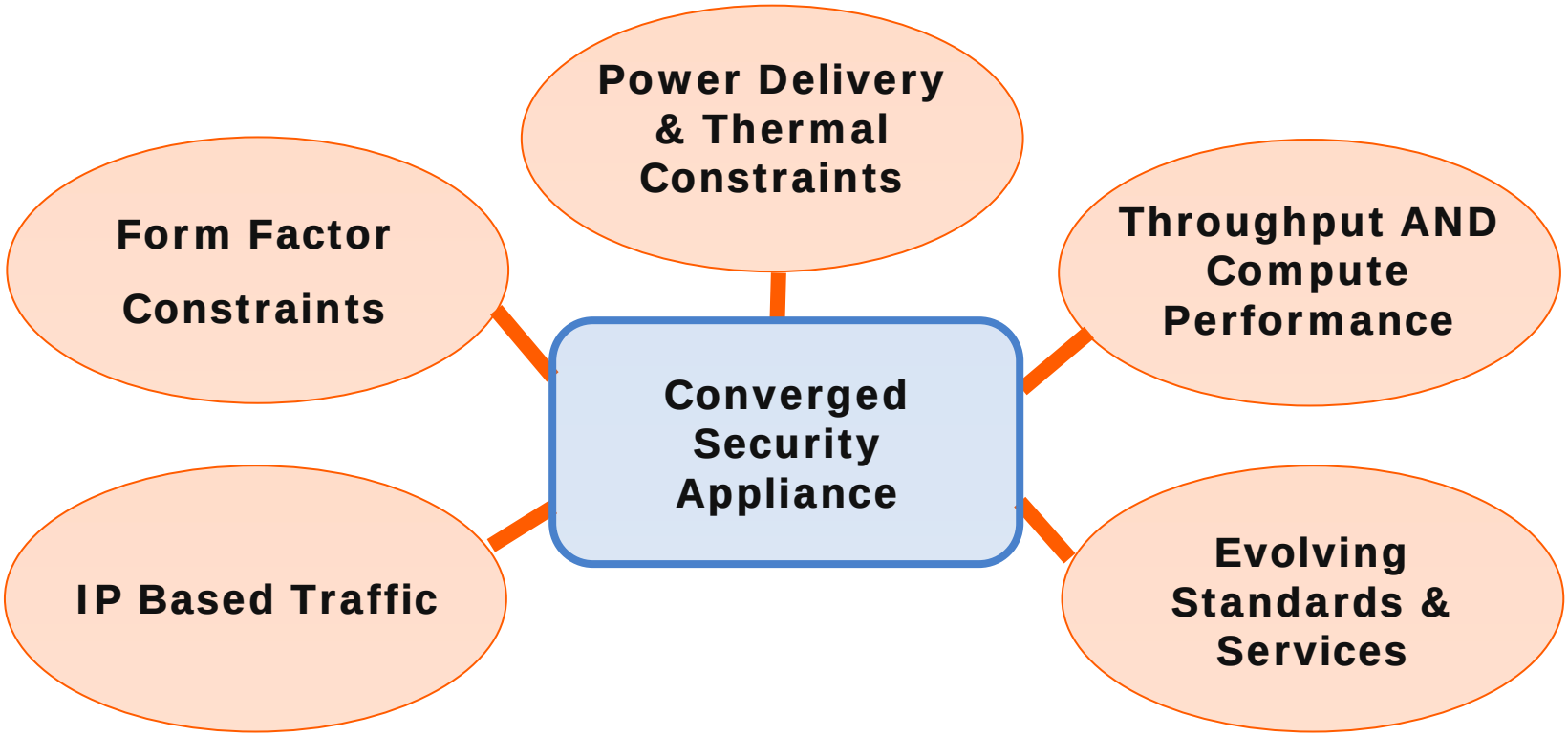
Eliminates Multiple Inefficient Point Products

Emerging SME Solution

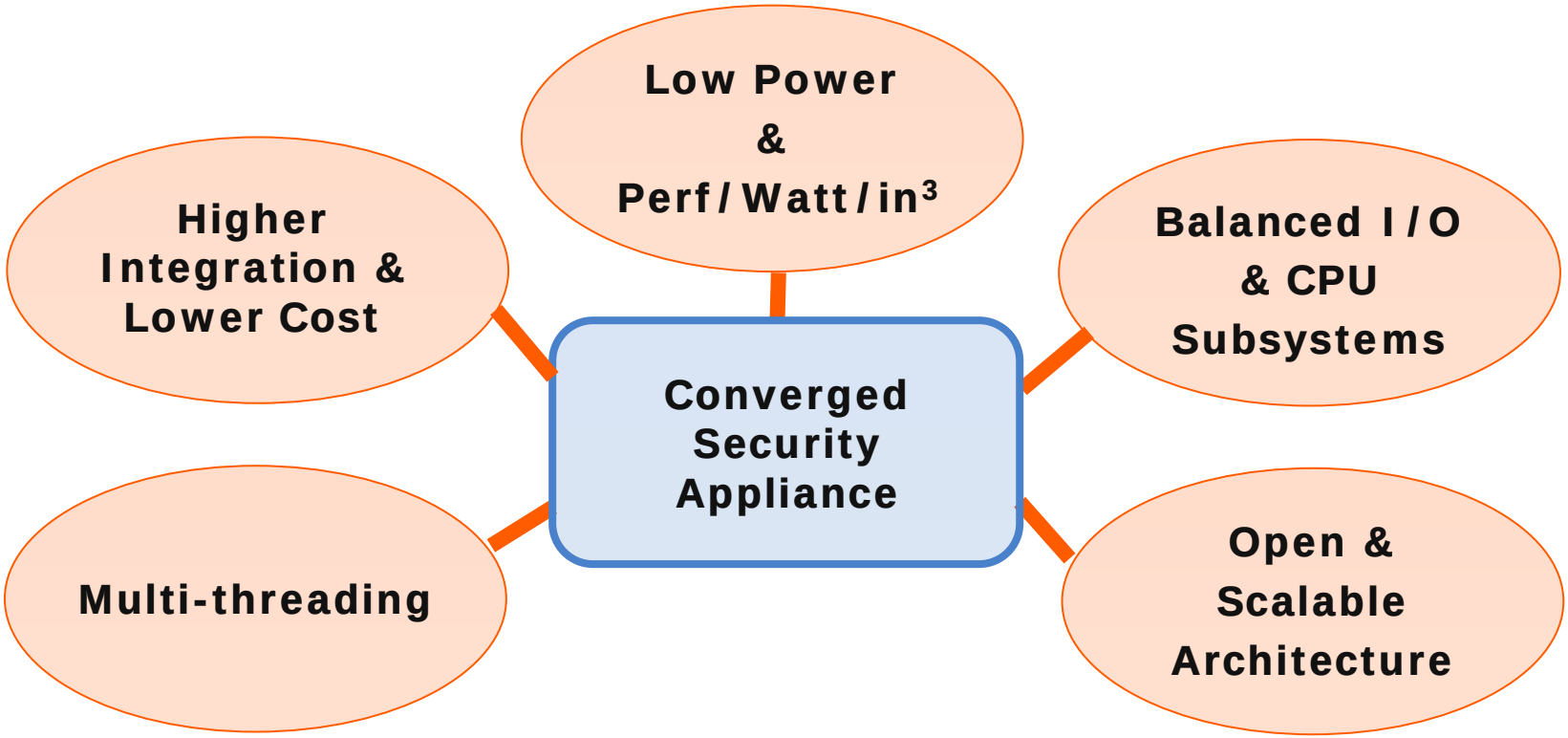


Result: ✓Cost-Effective ✓Simple ✓Scales

Converged Appliance: Requirements



Desired Product Architecture



Desired SME Solution: Affordable Features Today → Scalable for Future

Intel® QuickAssist Technology Introduction

Encompasses Industry Hardware Solutions

Future Intel Processor Integration of Accelerators

Software Architecture, Libraries, Industry APIs & Tools For Acceleration

Comprehensive Approach To Acceleration

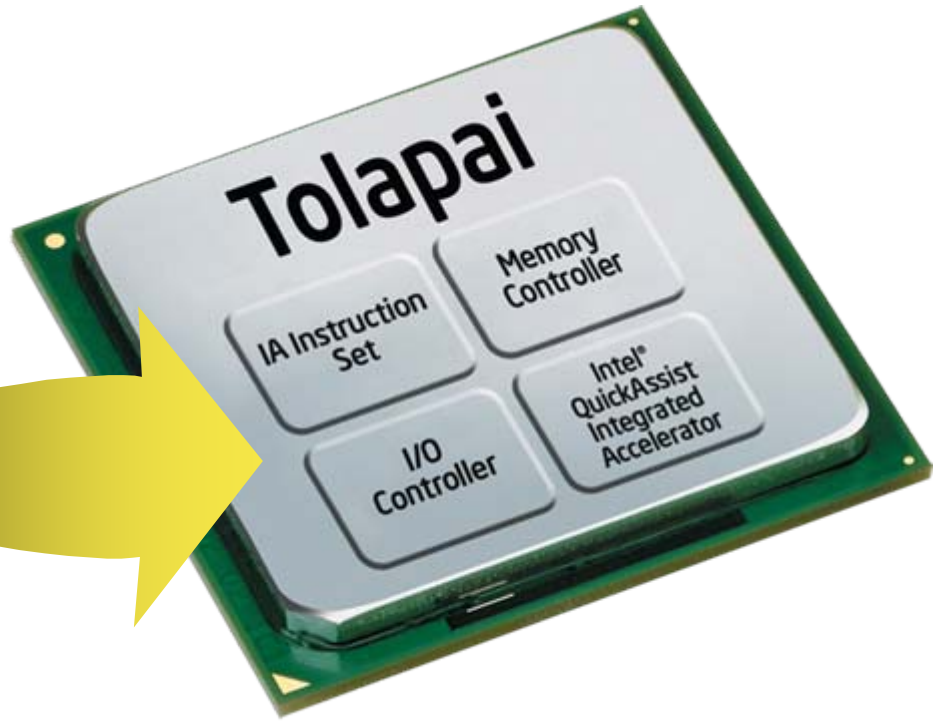
Introducing…Tolapai

Intel® Architecture Attributes

- General purpose Scalability
- Economies of Scale
- Software Infrastructure

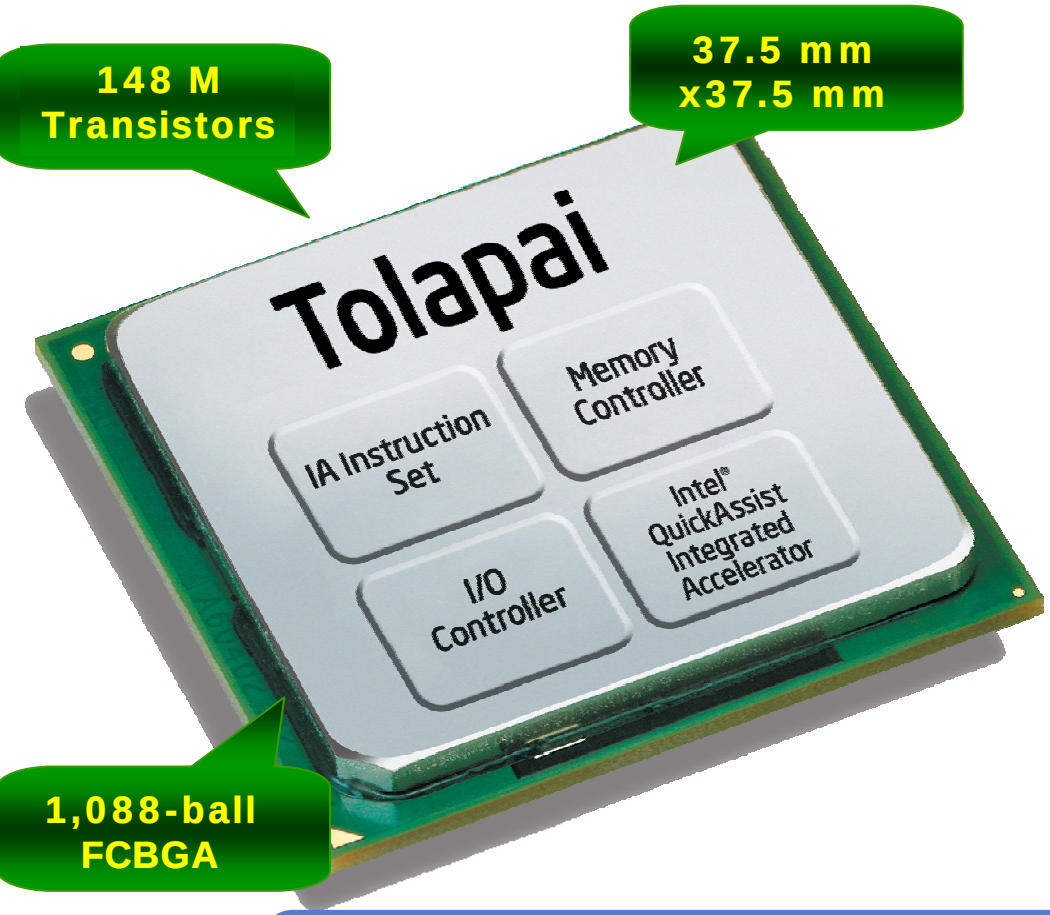
Intel® QuickAssist Integrated Accelerator

- Packet Processing
- Security Processing



Tolapai: ✓TTM ✓Power Efficient Performance ✓BOM cost

Tolapai: Integration Highlights

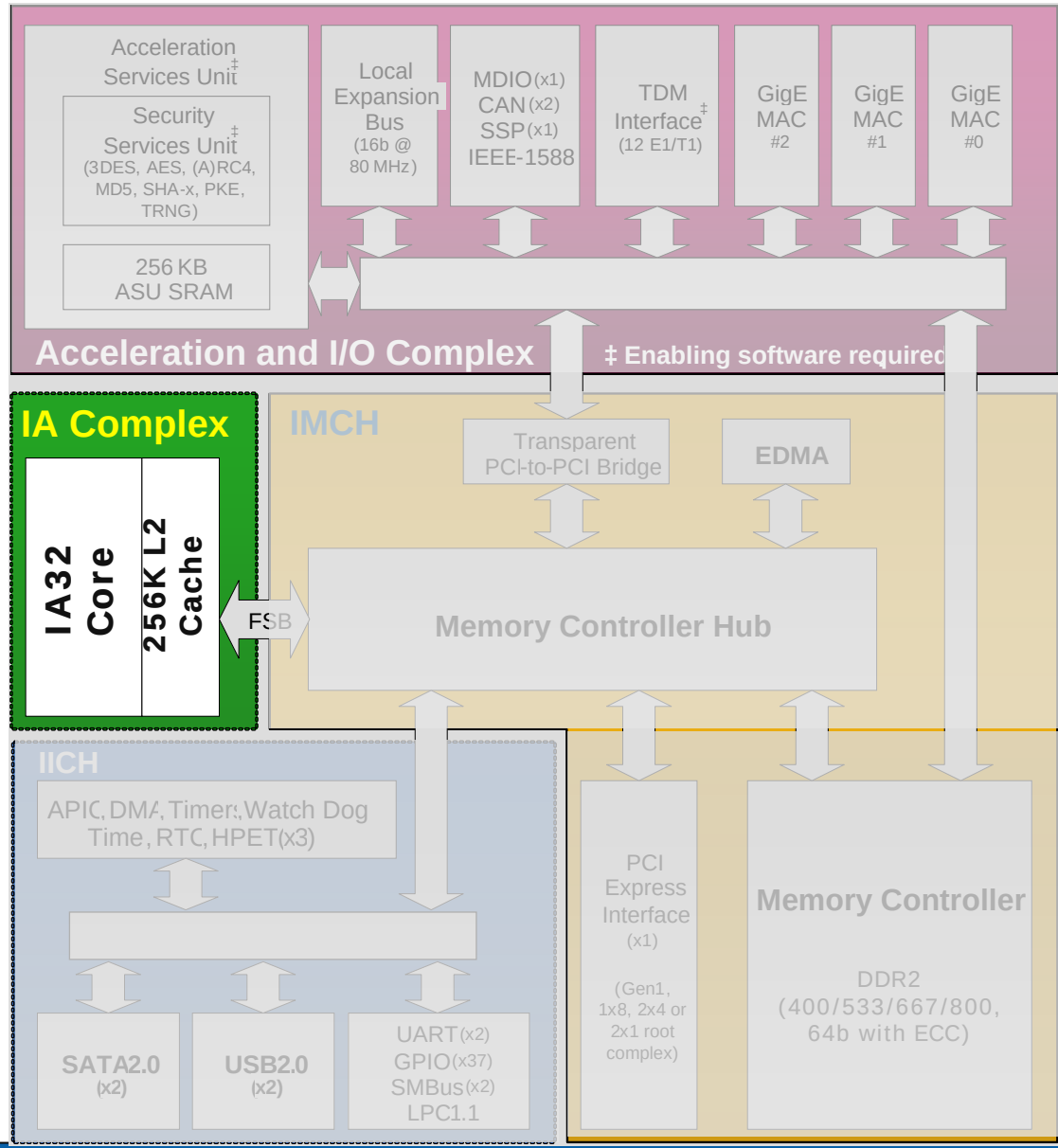


- IA CPU @ 600, 1066 and 1200MHz
- DDR2 memory controller (MCH)
- PCI Express*
- Standard IA PC peripherals (ICH)
- 3x Gigabit Ethernet MACs
- 3x TDM high-speed serial interfaces for 12 T1/E1 or Slic/Codec connections
- Intel® QuickAssist Integrated Accelerator
  - For security and IP telephony applications

Intel's first integrated IA CPU, chipset and memory controller since 1994's 80386EX.

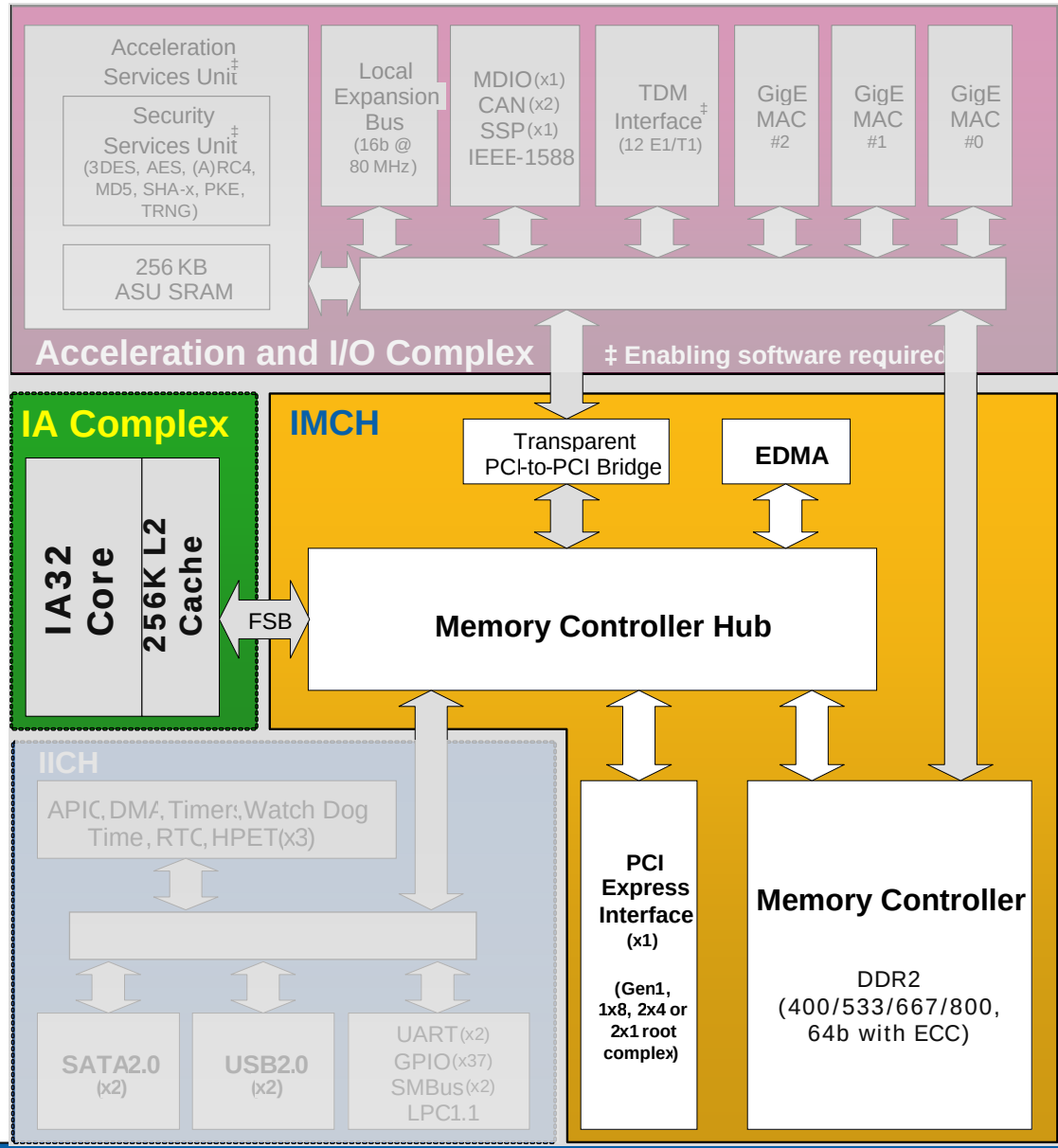
Details

- **IA CPU Core w/ 256KB L2 cache**
  - Intel® Pentium® M processor derivative
  - Power efficient



Details

- **IA CPU Core w/ 256KB L2 cache**
  - Intel® Pentium® M processor derivative
- **Integrated Memory Controller**
  - 1 channel 64-bit DDR2
  - 4 channel DMA engine
  - PCI Express* (1x8, 2x4, or 2x1)



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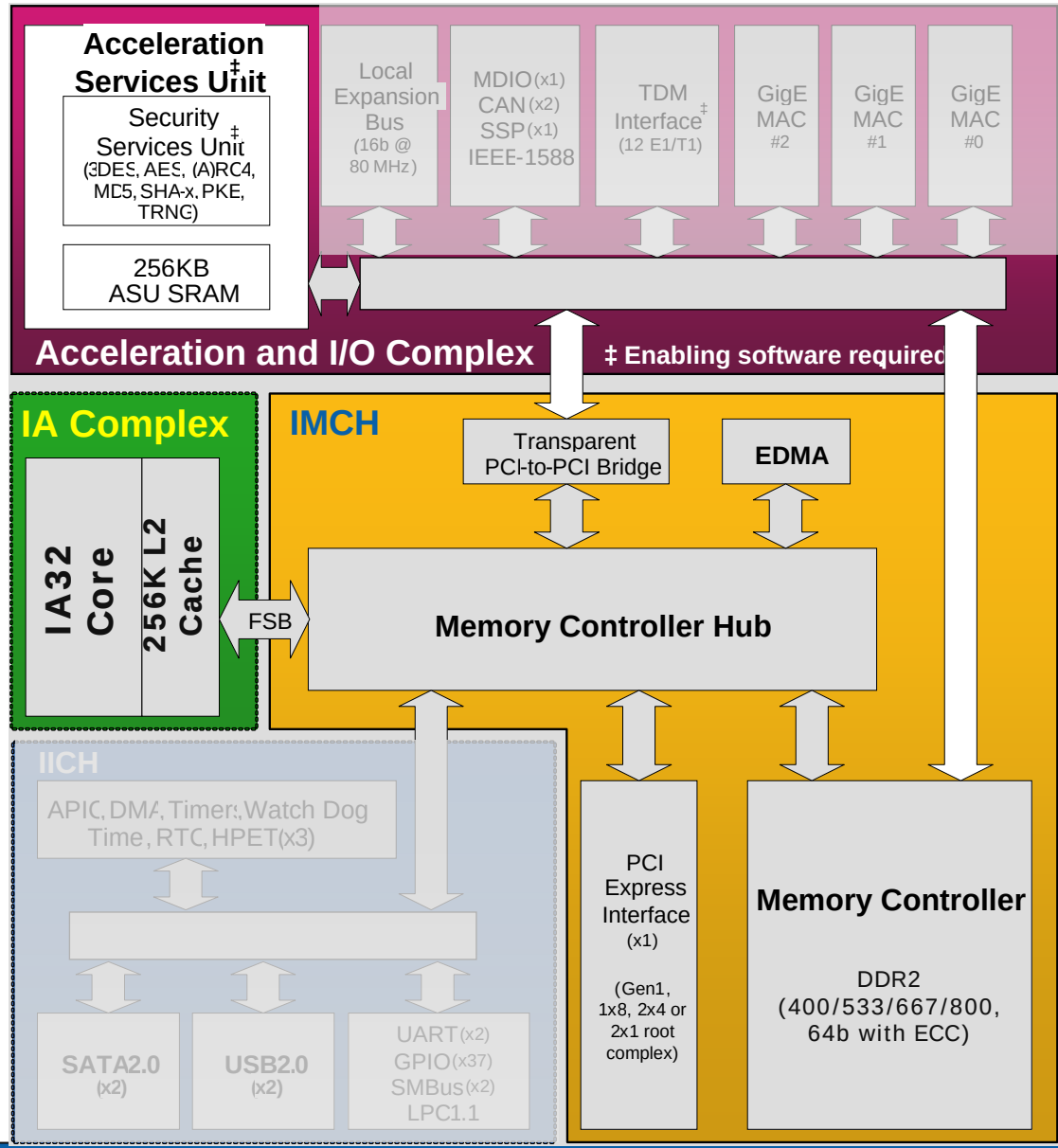
- **Intel® QuickAssist Acceleration**
  - Multi-core, Multi-threaded Engines
  - 256KB Internal SRAM
  - Security Hardware Acceleration for
    - Bulk: AES, 3DES, (A)RC4
    - Hash: MD5, SHA-x
    - Public Key – RSA, DSA, DH
    - Internal True Random Number Generator (TRNG)



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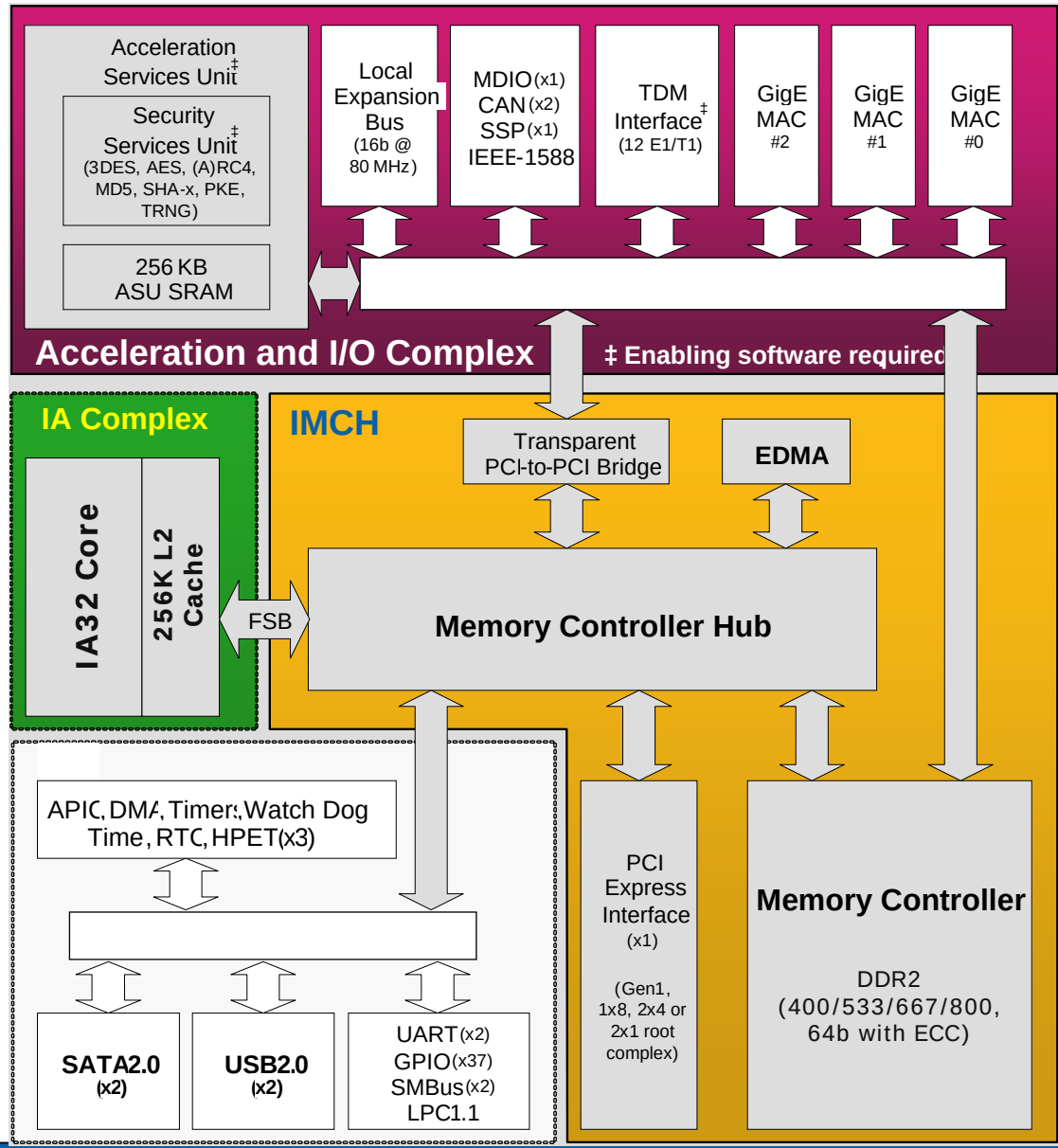
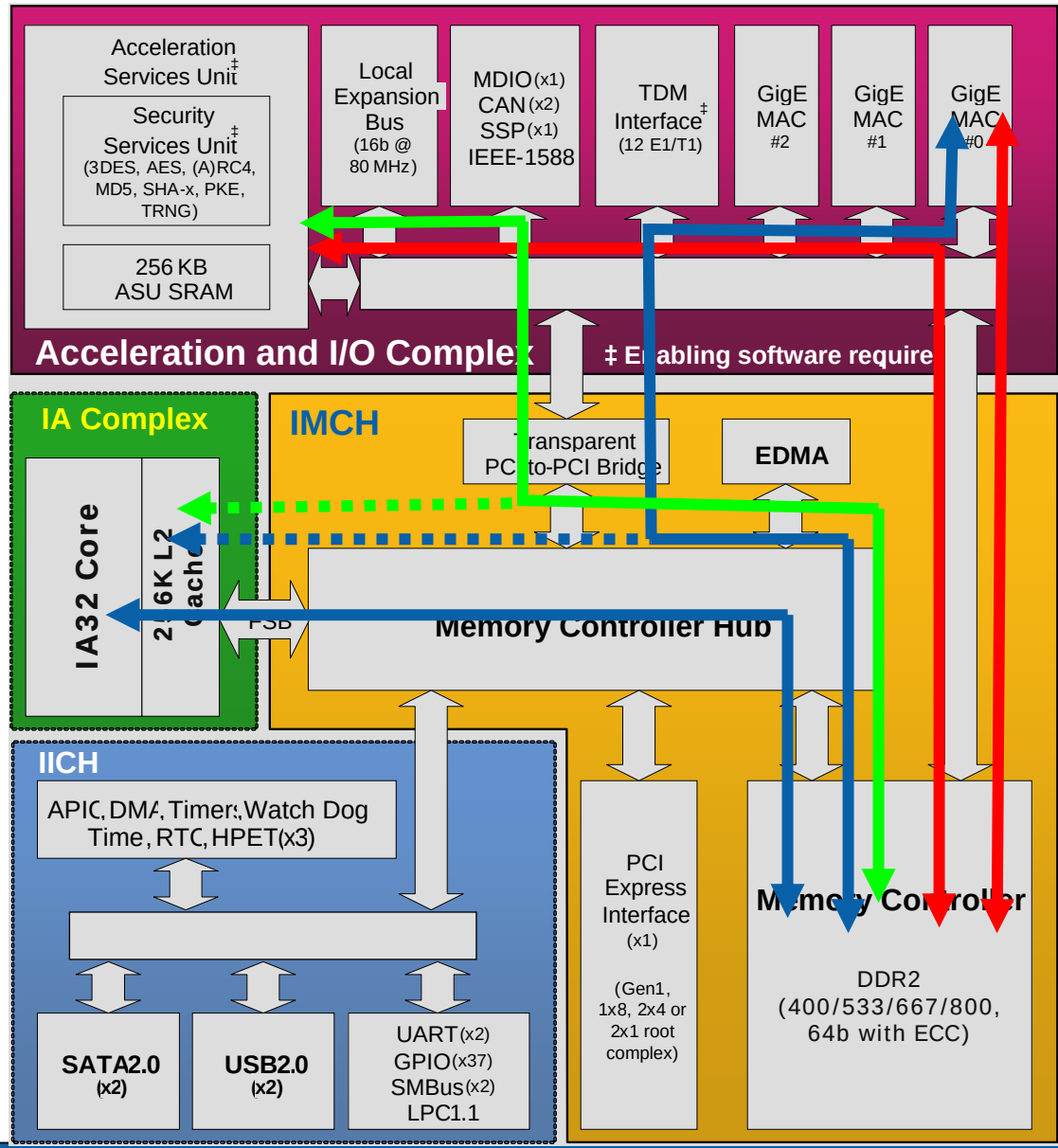
- **Integrated I/O Interfaces**
  - 3x TDM (12 T1/E1)
  - 3x GbE MAC (RGMII or RMII)
  - 1x Local Expansion Bus (16b)
  - 2x Controller Area Network (CAN)
  - 1x Sync Serial Port (SSP)
  - 2x UART, 37x GPIO,
  - 2x SMBus/I2C, LPC
  - 2x USB, 2x SATA
  - WDT, RTC



Packet Processing Flows

- **Classic IA (blue)**
  - GigE Rx DMA packets to DRAM (includes IA snoop)
  - IA interrupt
  - IA CPU runs protocol
  - IA CPU controls GigE TX
- **Fastpath (red)**
  - GigE Rx DMA packets to DRAM
  - Interrupt routed to accelerator
  - Accelerator operates on packet
  - Forwarding/filtering and security functions can be handled w/o IA CPU intervention
  - Accelerator controls GigE Tx
- **Exception Packets (green)**
  - Move packet to coherent DRAM (includes IA snoop)
  - Accelerator signals IA CPU



How IA and Accelerators share Memory

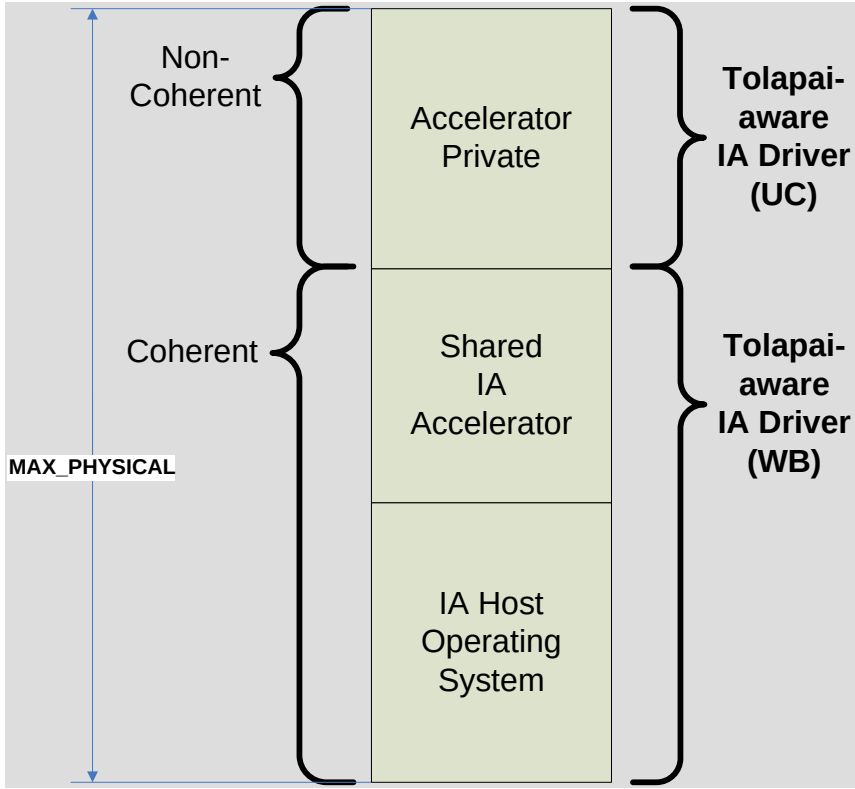
Accelerators run in physical address space

- Appear as a PCI device
- Run concurrently, async. to IA CPU
- IA CPU could be sleeping/throttled

IA and Accelerators share DRAM → Most Cost Effective

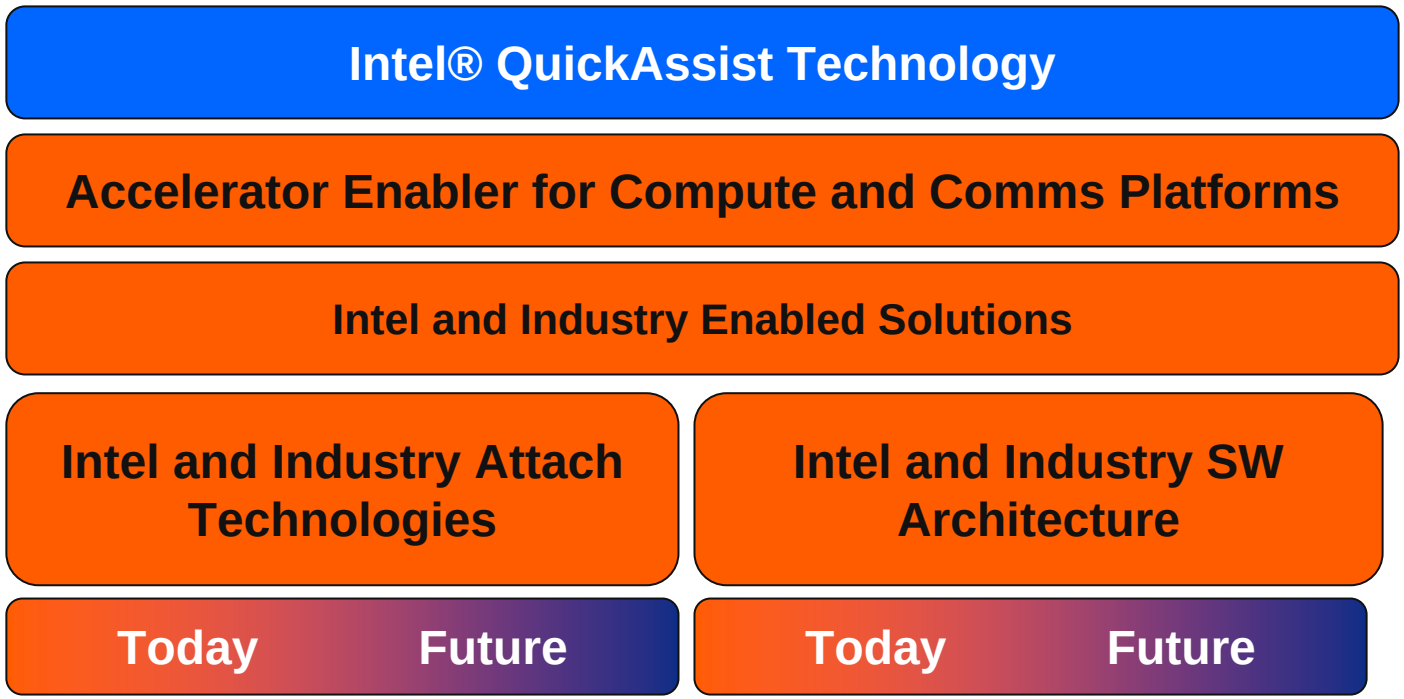
DRAM Partitioned

- Non-Coherent (Not Snooped)
  - Private to Accelerator
  - Physically contiguous portion hidden from OS
  - Accessible to Tolapai-aware IA driver
  - Separate high performance data path
- Coherent (Snooped)
  - Shared physical address space with IA

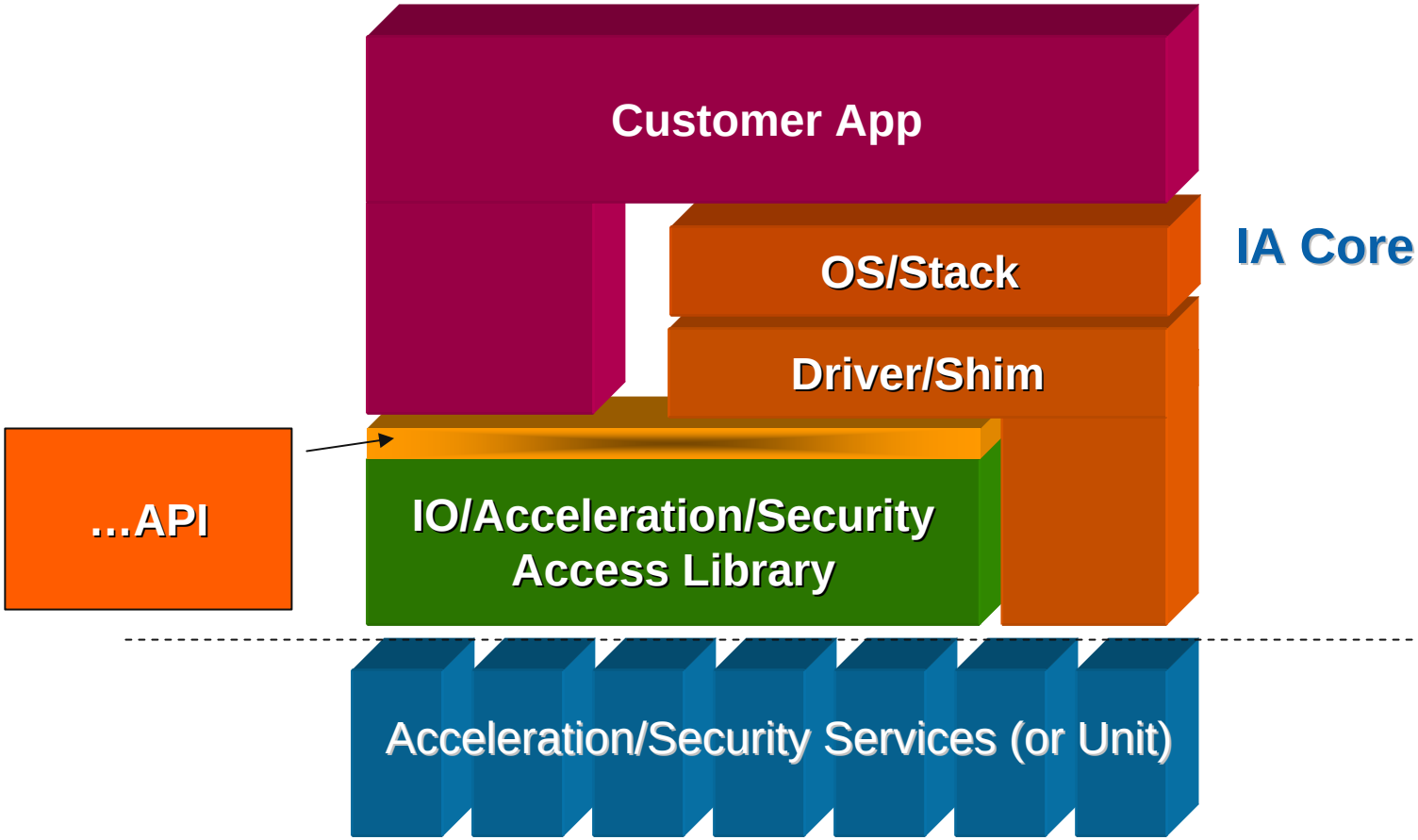


Tolapai Advantage: It's IA; Accelerators provide Power Efficient Performance; Innovative Integration enables cost effective, small FF solutions.

Intel® QuickAssist Technology Model

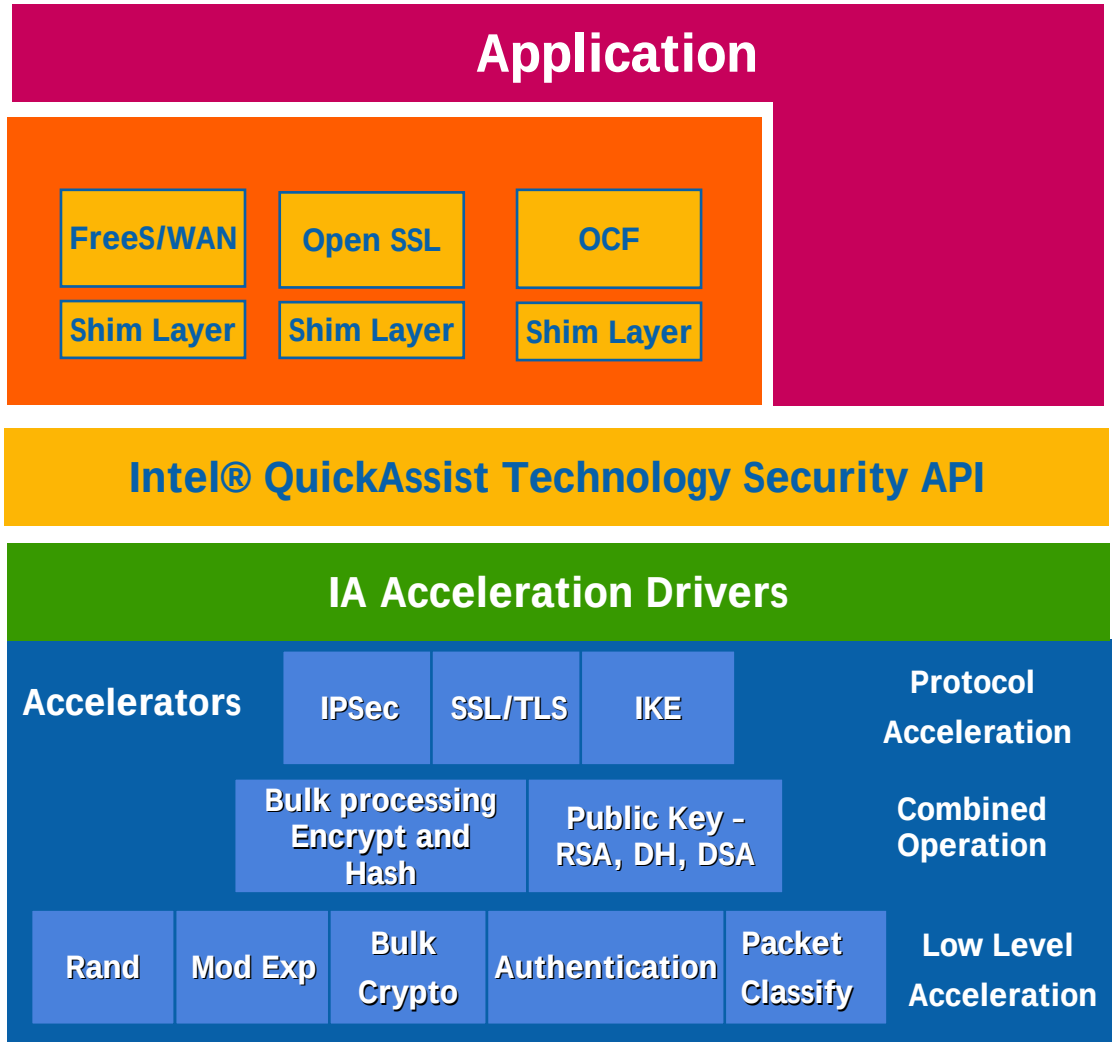


High Level SW Model



Tolapai Software Framework Goal: Enable Scalable Software Solutions

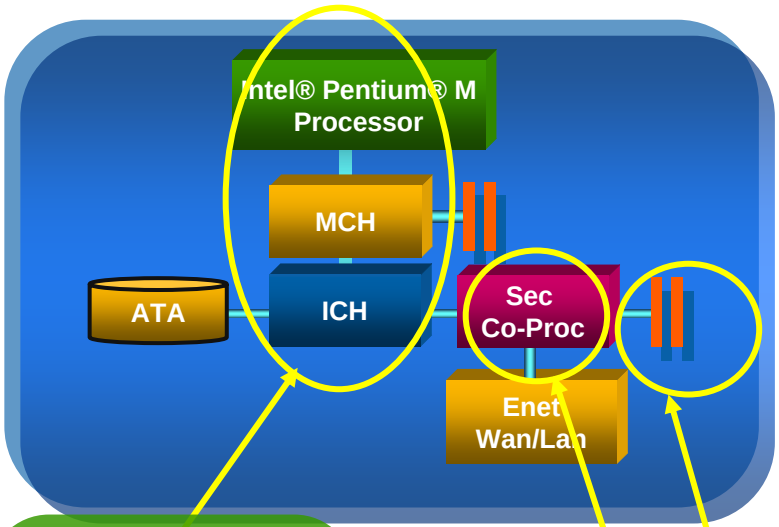
Security – Look aside Package



- Drivers for Linux* (Red Hat) and FreeBSD
- Intel® QuickAssist Technology Security API
  - Low level crypto API – PKCS #11 compliant
  - High level protocol support
- Integrated with middleware frameworks
  - OpenSSL
  - OCF
  - FreeS/WAN, etc.

Typical Application – SMB VPN/Firewall

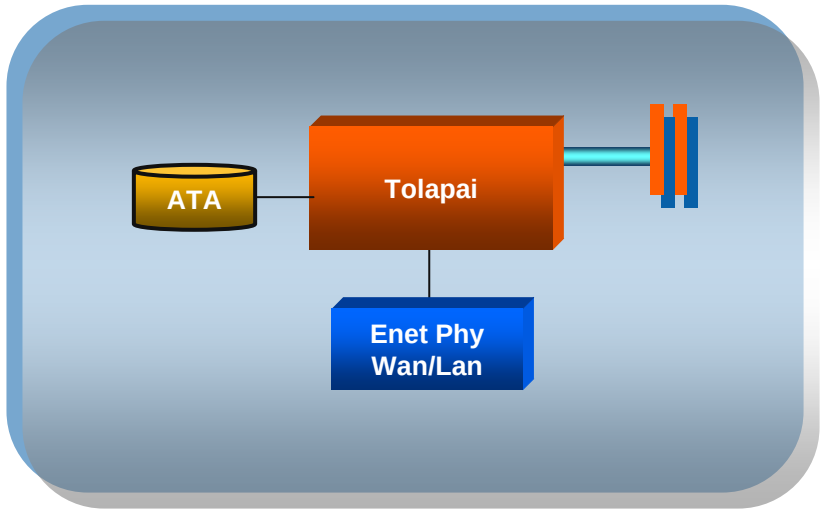
Current Equiv Solution



Additional Area, Cost, Core Utilization, Architecture - Lookaside Only

Additional Area, Cost

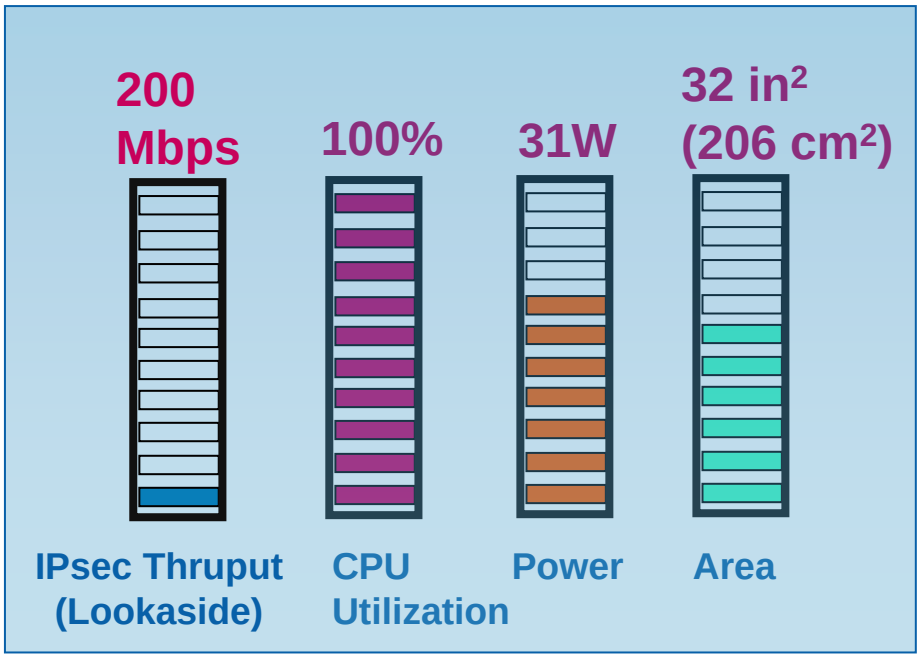
Tolapai

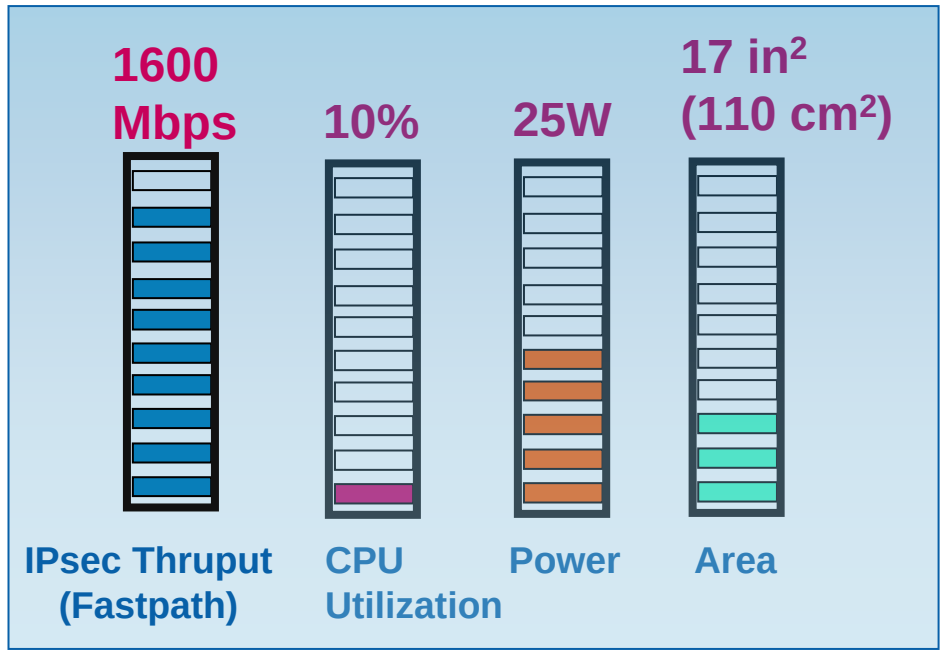


- IA SoC optimized for Power/Performance
- In-line network/security acceleration
- Integrated I/O devices
- IA SW compatibility
- Highest Compute Cycles Available/$

Expected Tolapai Benefits

Example - IPSec VPN Appliance using Tolapai





Traditional 4-chip IA Solution
(CPU + MCH + ICH + PCI Crypto Accelerator)

1-chip Tolapai Solution
(simulated)

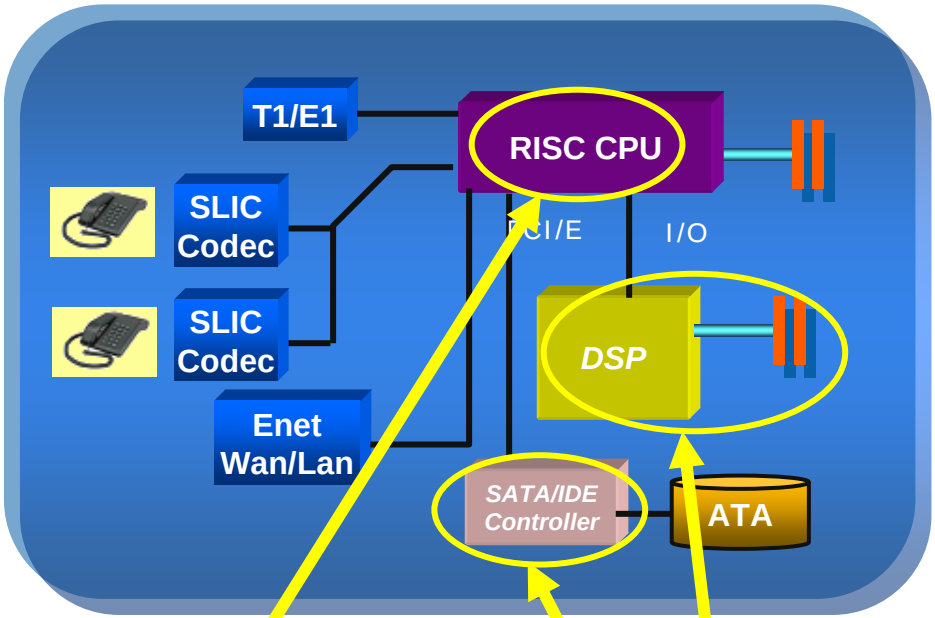
Assumptions:

- Compares Intel® Pentium® M processor-based platform with external PCI crypto accelerator to 1-chip Tolapai solution
- 256 byte packets with 2048 IPsec VPN tunnels

Tolapai = Intel® embedded processor for 2008.

Typical IP Telephony Application – Converged IP PBX with Firewall

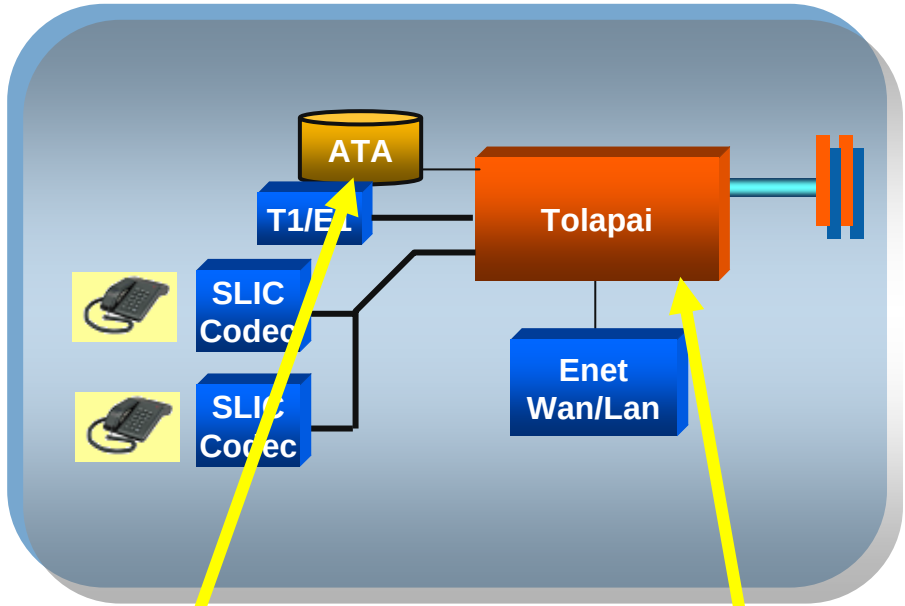
Current Equiv Solution



Low Perf; Little App Headroom

Additional Cost, Area, Power

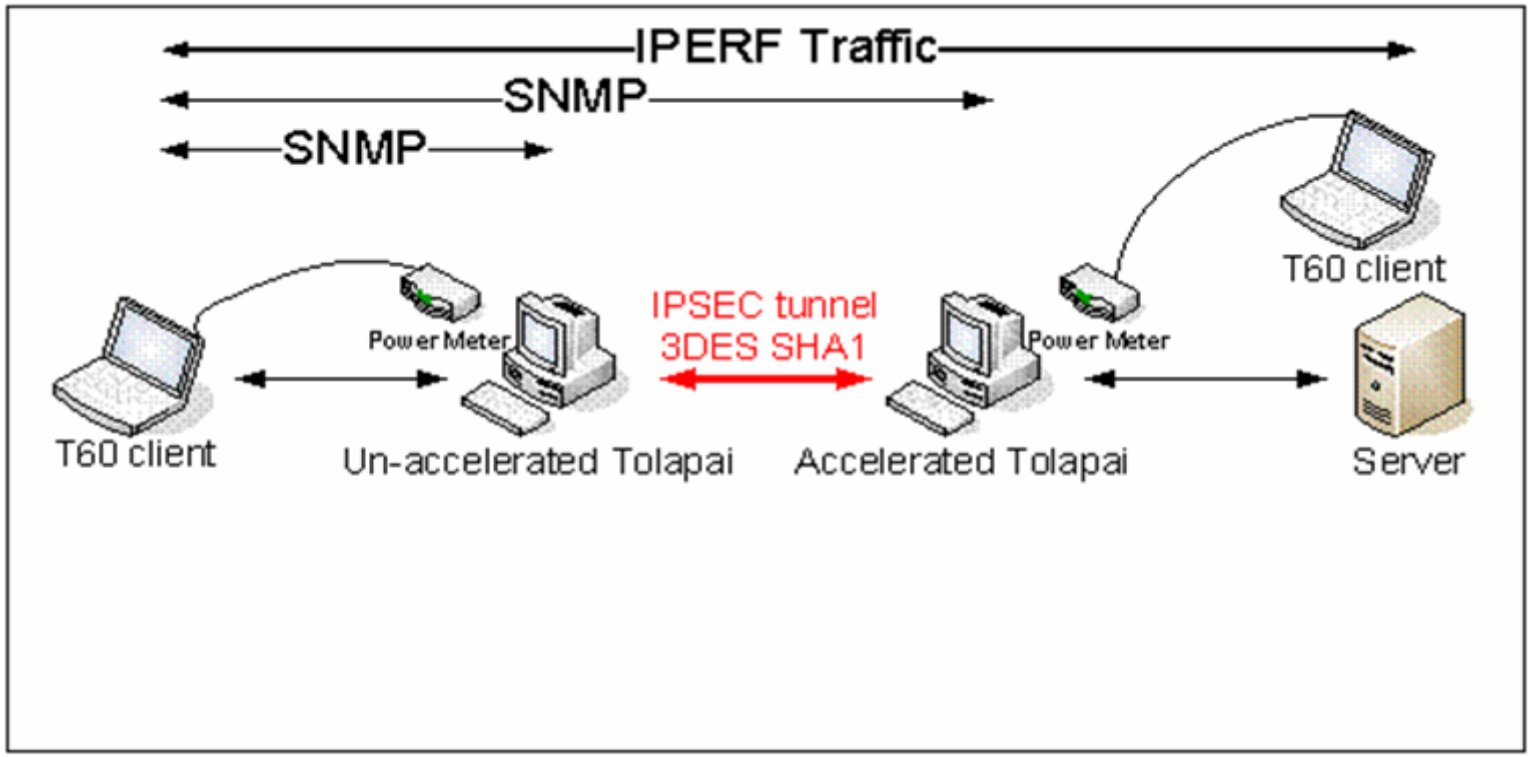
Tolapai



Storage for VM Solutions

IPP SW Handles Echo Cancel, Vocoding, Signaling

Tolapai Demo



Tolapai offers a cost effective, faster TTM, software scalable and “Power efficient Performance” solution for SME Security and Voice Appliances

Summary

- Desired SME Solution: Affordable Features Today → Scalable for Future
- Tolapai Advantage: It's IA; Accelerators provide Power Efficient Performance; Innovative Integration enables cost effective, small FF solutions
- Tolapai Software Framework Goal: Enable Scalable Software Solutions
- Tolapai offers a cost effective, faster TTM, software scalable and "Power efficient Performance" solution for SME Security and Voice Appliances and generic Embedded segments

Additional sources of information:

- Tolapai for Small and Medium Enterprises – Animation: www.intel.com/go/soc
- Other Sessions / Chalk Talks / Labs –
  - QATS004 - Geneseo and Intel® QuickAssist Technology Architecture Overview
  - QATS003 - Accelerator Exoskeleton: Intel® Architecture Look and Feel for Heterogeneous Cores
  - QATS001 - Intel® Embedded Processor for 2008 (Tolapai) SoC Architecture Overview
  - QATS002 - Intel® QuickAssist Technology FSB-FPGA Accelerator Architecture
  - QATL001 - PCIe 2.0 Interop Lab
  - QATC001 - Geneseo and Intel® QuickAssist Technology Architecture Chalk Talk by Intel Fellow Ajay Bhatt
  - QATP001 - Industry Panel: Trends and challenges ahead for accelerator usage and growth
- Accelerators in Action : Visit the I/O & Application Acceleration Community in the showcase to see technology demonstrations from Intel and other industry-leading companies
- More web based info: http://www.intel.com/technology/platforms/quickassist
- This Session presentation (PDF) is available from www.intel.com/idf. Some sessions will also provide Audio-enabled presentations after the event.

Call to Action

Please contact your local Intel Sales Representative for more information on Tolapai and associated product collateral.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