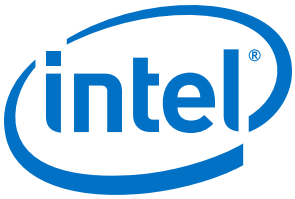


Intel® Core™ i7 Processor Family for the LGA2011-3 Socket

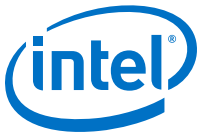
Thermal/Mechanical Specification and Design Guide (TMSDG)

Supporting Desktop Intel® Core™ i7-5960X Extreme Edition Processor for the LGA2011-3 Socket

Supporting Desktop Intel® Core™ i7-59xx and i7-58xx Processor Series for the LGA2011-3 Socket

August 2014

Order No.: 330842-001



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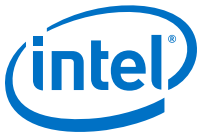
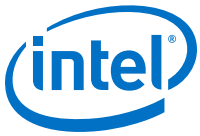


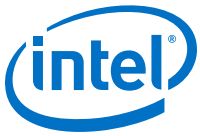
Revision History

Revision Number	Description	Date
001	Initial Release	August 2014

Contents



Figures



Tables

1.0 Introduction

This document provides specifications and guidelines for the design of thermal and mechanical solutions for Intel® Core™ i7 Processor Family for the LGA2011-3 Socket. The processors covered are listed in the Processor Datasheet, Volume 1 (see Reference Documents).

Note: When information in this document is applicable to all products this document will use 'processor' or 'processors' to simplify this document.

The components and information described in this document include:

- Thermal profiles and other processor specifications and recommendations
- Processor Mechanical load limits
- Independent Loading Mechanism (ILM) specifications and recommendations
- Heatsink recommendations
- Reference designs for processor thermal solution (heatsink) and associated retention hardware
- Reference designs for the socket, ILM and associated back plate

The goals of this document are:

- To assist board and system thermal mechanical designers
- To assist designers and suppliers of processor heatsinks

1.1 Reference Documents

Document Title	Document Number
Intel® Core™ i7 Processor Family for the LGA2011-3 Socket Datasheet - Volume 1 of 2	330839
Intel® Core™ i7 Processor Family for the LGA2011-3 Socket Datasheet - Volume 2 of 2	330840

2.0 LGA2011-3 Socket Overview

This section describes a surface mount, LGA (Land Grid Array) socket intended for the Intel® Core™ i7 Processor Family for the LGA2011-3 Socket processor-based platform. The socket provides I/O, power and ground contacts for processor operation. The socket contains 2011 contacts arrayed about a cavity in the center of the socket with lead-free solder balls for surface mounting on the motherboard.

The LGA2011-3 uses a hexagonal area array ball-out which provides many benefits:

- Socket contact density increased by 12% while maintaining 40 mil minimum via pitch requirements. as compared to a linear array
- Corresponding square pitch array's would require a 38mil via pitch for the same package size.

LGA2011-3 has 1.016 mm (40 mil) hexagonal pitch in a 58x43 grid array with 24x16 grid depopulation in the center of the array and selective depopulation elsewhere.

Figure 1. Hexagonal Array in LGA2011-3

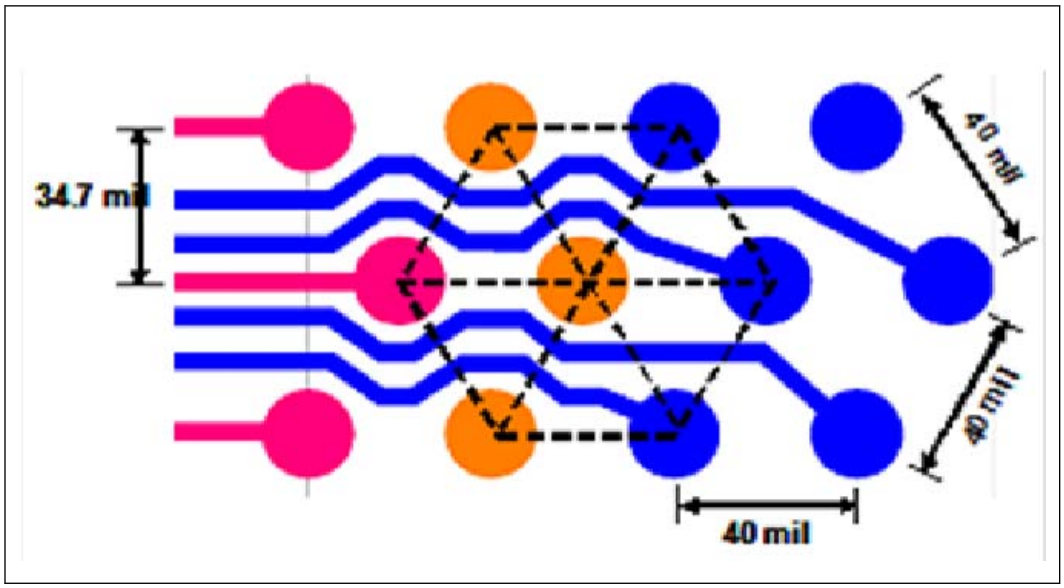


Table 1. LGA2011-3 Socket Attributes

LGA2011-3 Socket	Attributes
Component Size	58.5 mm (L) X 51 mm (W)
Pitch	1.016 mm (Hex Array)
Ball Count	2011

The socket must be compatible with the package (processor) and the Independent Loading Mechanism (ILM). Internal keying posts ensure socket processor compatibility. An external socket key ensures ILM and socket compatibility. The ILM reference design includes a back plate; an integral feature for uniform loading on the socket solder joints and contacts.

2.1 Socket Components

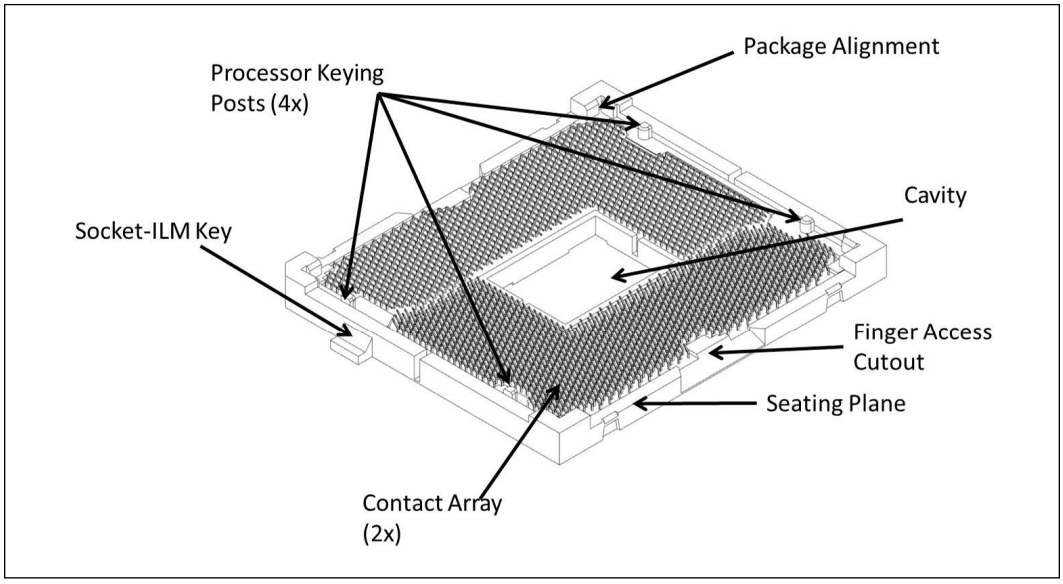
The socket has two main components, the socket body: composed of a housing solder balls, and processor contacts, and Pick and Place (PnP) cover. The socket is delivered as a single integral assembly. Below are descriptions of the integral parts of the socket.

Socket Body Housing

The housing material is thermoplastic or equivalent with UL 94 V-0 flame rating capable of withstanding 260°C for 40 seconds (typical reflow/rework). The socket coefficient of thermal expansion (in the XY plane), and creep properties, are such that the integrity of the socket is maintained for the environmental conditions listed in the TMSDG.

The color of the housing will be dark as compared to the solder balls to provide the contrast needed for pick and place vision systems. A labeled representation of the socket can be seen in the figure below.

Figure 2. Socket with Labeled Features



Solder Balls

A total of 2011 solder balls corresponding to the contacts are on the bottom of the socket for surface mounting with the motherboard.

The socket has the following solder ball material:

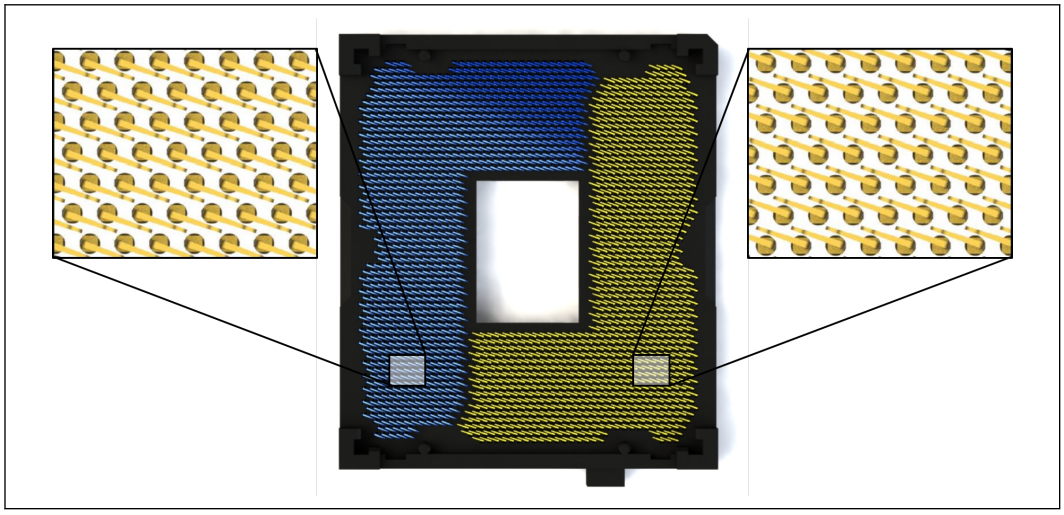
- Lead free SAC305 (SnAgCu) solder alloy with a silver (Ag) content 3%, copper (Cu) 0.5%, tin (Sn) 96.5% and a melting temperature of approximately 217°C. The immersion silver (ImAg) motherboard surface finish and solder paste alloy must be compatible with the SAC305 alloy solder paste.

Contacts

The base material for the contacts is high strength copper alloy. For the area on socket contacts where processor lands will mate, there is a 0.381 mm [0.015 inches] minimum gold plating over 1.27 mm [0.05 inches] minimum nickel underplate. No contamination by solder in the contact area is allowed during solder reflow. All socket contacts are designed such that the contact tip lands within the substrate pad boundary before any actuation load is applied and remain within the pad boundary at final installation, after actuation load is applied.

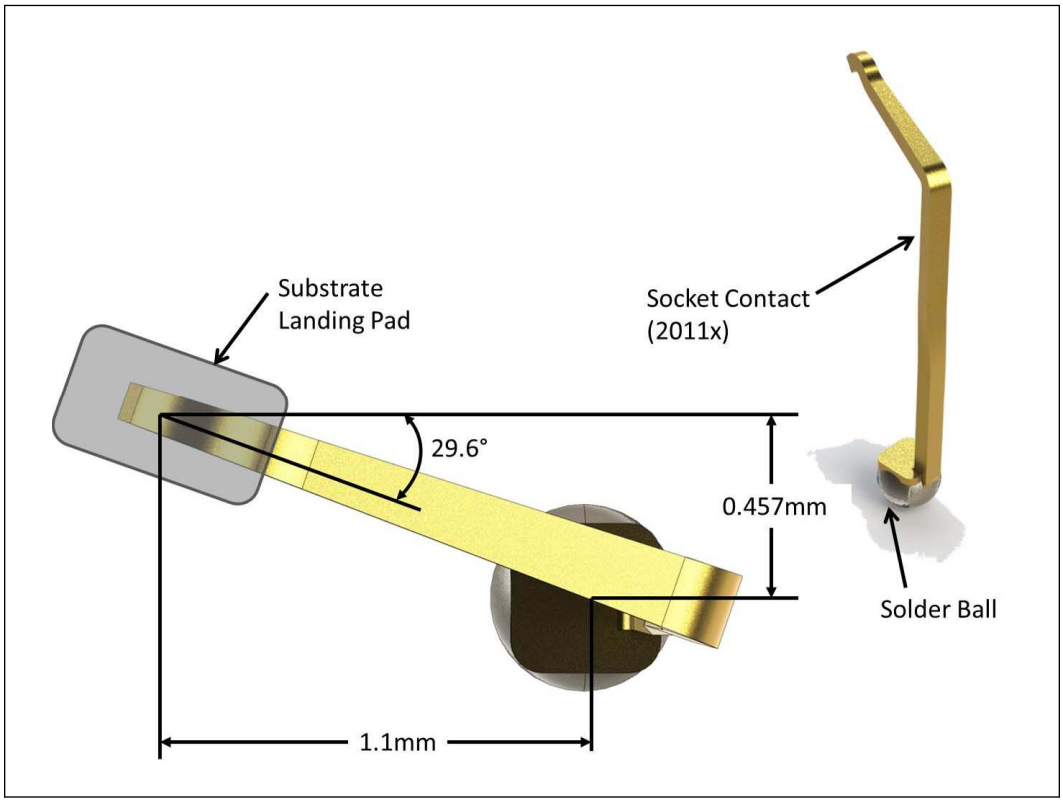
The contacts are laid out in two L-shaped arrays as shown in the figure below. The detailed view of the contacts indicate the wiping orientation of the contacts in the two regions to be 29.6°.

Figure 3. Contact Wiping Direction



The contact between substrate land and socket contact are offset. The following diagram shows contact offset from solder ball location and orientation of contact tip.

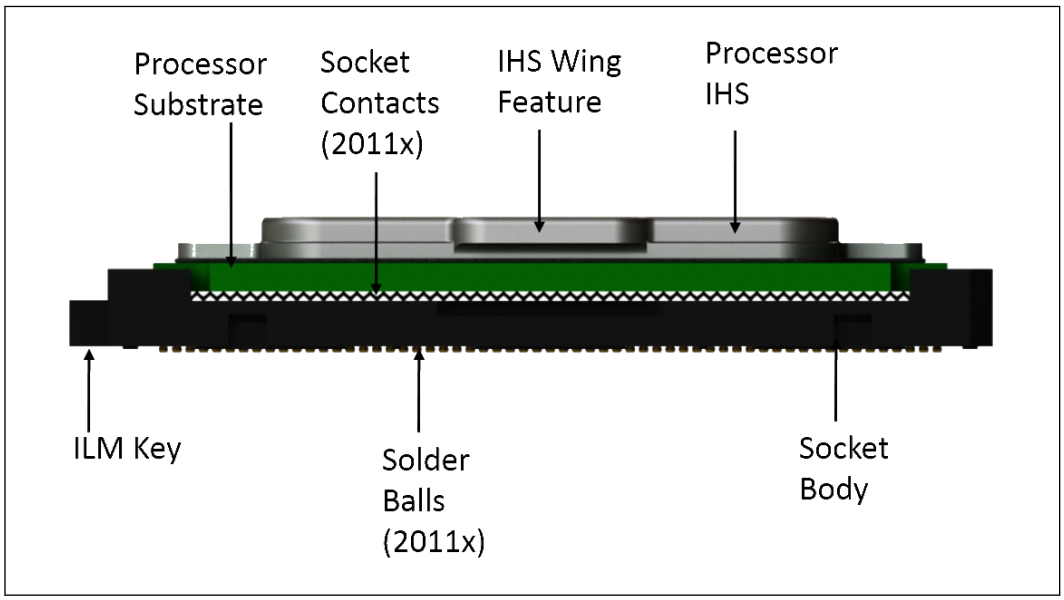
Figure 4. Contact Tip Offset with Respect to Solder Ball



Socket Standoffs

Standoffs on the bottom of the socket base establish the minimum socket height after solder reflow. The following diagram highlights each feature of the socket-processor stack up.

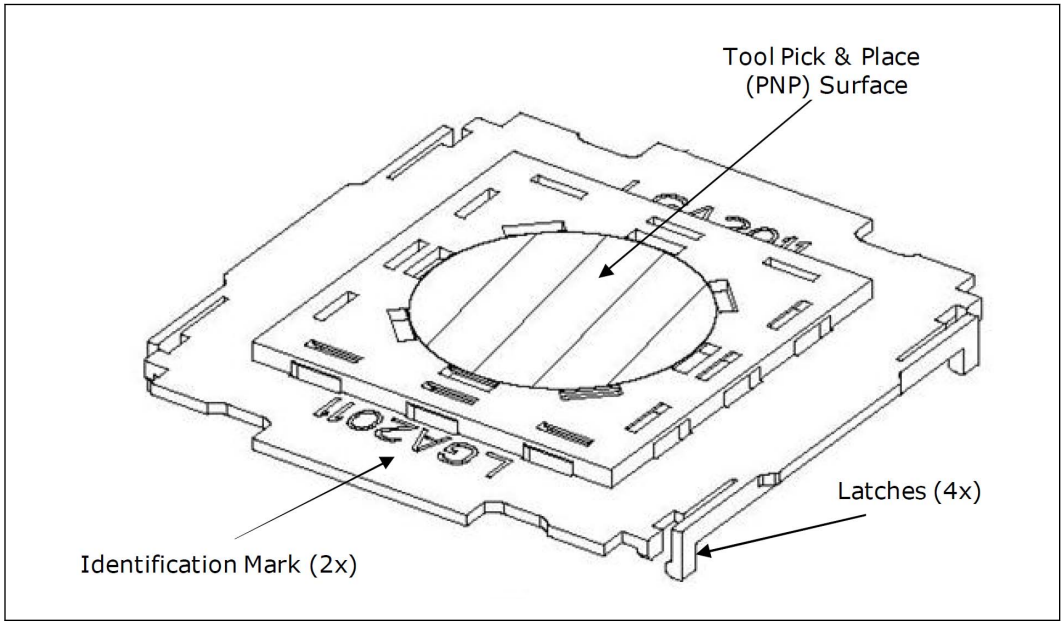
Figure 5. Processor Socket Stack Up



Pick and Place Cover

The cover provides a planar surface for vacuum pick up used to place components in the Surface Mount Technology (SMT) manufacturing line. The proceeding diagram labels key features of the Pick and Place cover.

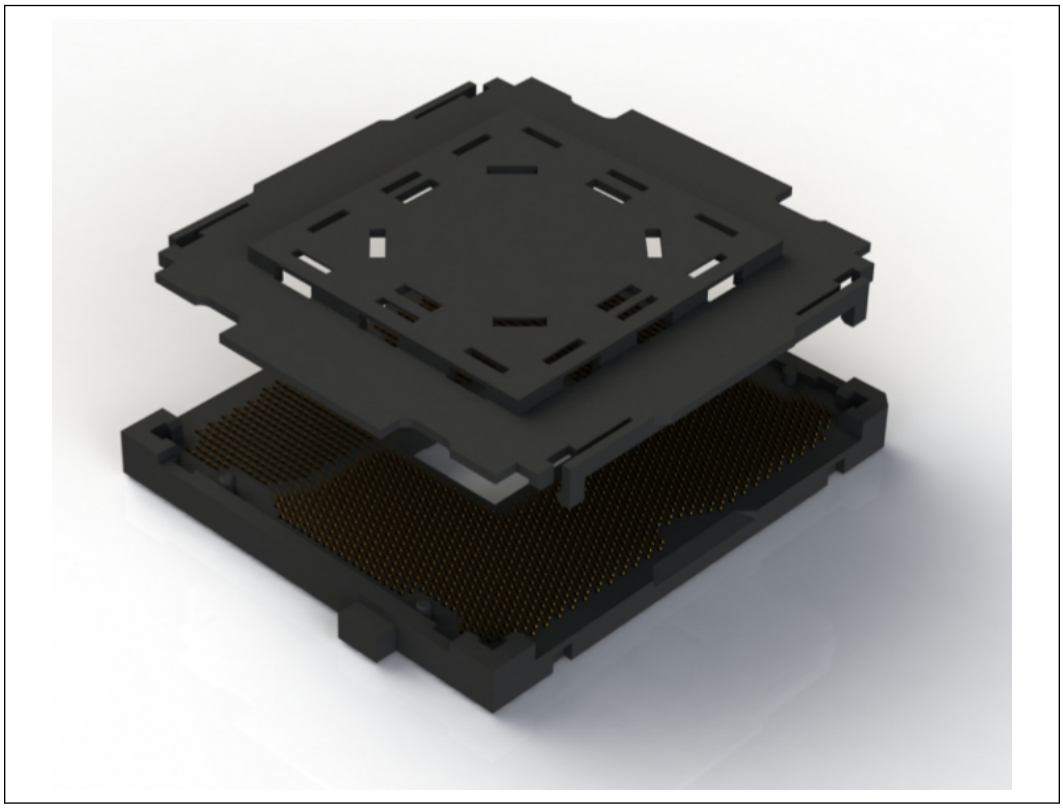
Figure 6. Pick and Place Cover with Labeled Features



The cover remains on the socket during reflow to help prevent contamination during reflow. The cover can withstand 260°C for 40 seconds (typical reflow/rework profile) and the environmental conditions listed in the TMSDG.

The following figure diagrams the PnP and socket assembly. To reduce risk of damage to socket contacts the pick and place (PnP) cover remains on the socket during ILM installation.

Figure 7. PnP Cover and Socket Assembly



Once the ILM with its cover is installed Intel is recommending the PnP cover be removed to help prevent damage to the socket contacts. To reduce the risk of bent contacts the PnP Cover and ILM Cover were designed to not be compatible. Covers can be removed without tools.

The pick and place covers are designed to be interchangeable between socket suppliers.

2.2 Socket Land Pattern Guidance

The land pattern guidance provided in this section applies to printed circuit board design. Recommendation for Printed Circuit Board (PCB) Land Patterns is to ensure solder joint reliability during dynamic stresses, often encountered during shipping and handling and hence to increase socket reliability.

LGA 2011-3 Land Pattern

The land pattern for the LGA2011-3 socket is 40 mils hexagonal array see the following figure for detailed location and land pattern type.

Note: There is no round-off (conversion) error between socket pitch (1.016 mm) and board pitch (40 mil) as these values are equivalent.

Figure 8. Socket 2011-3 Land Pattern

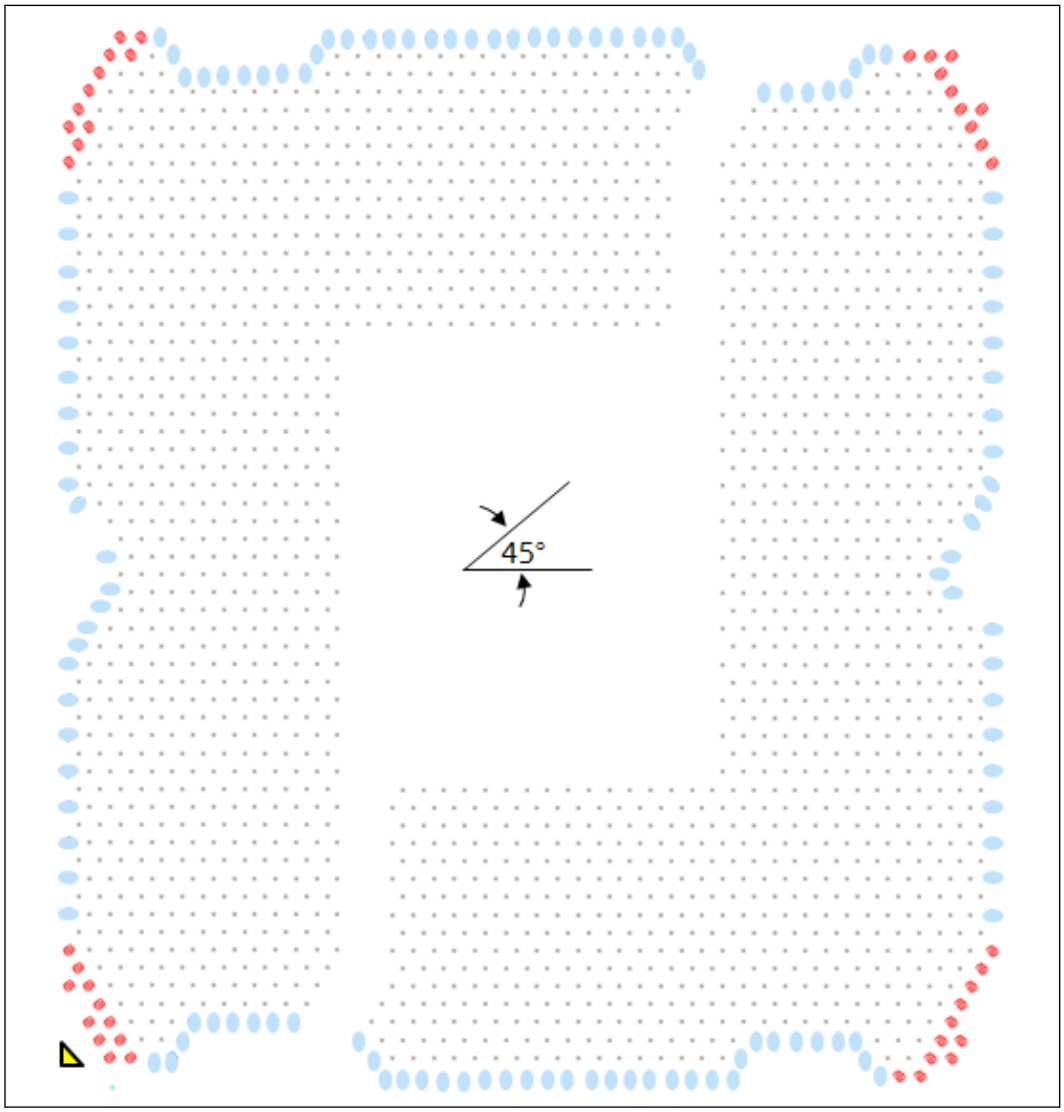


Table 2. PIN Count By Pad Definition

Pad Definition / Padstack	Color	Quantity
20 X 17 Oblong Partially SMD / O17X20	**RED Pins**	43
20 X 17 Oblong Partially SMD / O17X20	**LIGHT BLUE Pins**	123
17 mil Ø MD / C17	**GREY Pins**	1845

Notes:
1. **RED Pins:** Corner nCTF pads (43 total) are all designed as 20 X 17 mil oblong partially soldermask defined pads with an SRO of 17+/-1mil Ø (shown below). The long axis of the pad is oriented at 45° from the center of the socket. All nCTF pads require thick traces ideally oriented at 45° toward the package corner.
2. **LIGHT BLUE Pins:** Edge CTF pads (total) are all designed as 20 X 17 mil oblong partially soldermask defined pads with an SRO of 17+/-1mil Ø (shown below). The long axis of the pad is oriented at 90° to the socket edge.
3. **GREY Pins:** Critical to function pins are all designed as 17 mil circular MD (Metal Defined) pads.

2.3 Socket Loading Requirements

The socket must meet the mechanical loading and strain requirements outlined in the table below. All dynamic requirements are under room temperature conditions while all static requirements are under product use condition temperature. Specifically, ILM and HS load range may vary for different LGA 2011 derivatives (e.g. 2011-0, 2011-1) due to the package form factor, and the design of loading mechanism and thermal solution (e.g., HS mass).

2.3.1 Socket Loading Specifications

The table below provides load specifications for the socket. These mechanical limits should not be exceeded during component assembly, mechanical stress testing, or standard drop and shipping conditions. All dynamic requirements are under room temperature conditions while all static requirements are under 100 °C conditions.

Table 3. Socket Load Values

Parameter	Load Limits, SI Units		Load Limits, Imperial Units		Definition
	Min	Max	Min	Max	
Static Compressive per Contact	15 (gf)	38 (gf)	0.53 (ozf)	1.34 (ozf)	The compressive load applied by the package on the LGA contacts to meet electrical performance. This condition must be satisfied throughout the life of the product
Static Compressive (ILM)	445 (N)	712 (N)	100 (lbf)	160 (lbf)	The total load applied by the enabling mechanism onto the socket as transferred through the package, contacts and socket seating plane.
Static Compressive Beginning of Life (HS)	222 (N)	400 (N)	50 (lbf)	90 (lbf)	The total load applied by the heatsink mechanism onto the socket as transferred through the package, contacts and socket seating plane. Measured at Beginning of Life
Static Compressive End of Life (HS)	178 (N)	400 (N)	40 (lbf)	90 (lbf)	The total load applied by the heatsink mechanism onto the socket as transferred through the package, contacts and socket seating plane. Measured at End of Life

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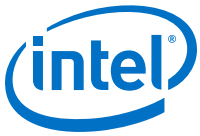


Parameter	Load Limits, SI Units		Load Limits, Imperial Units		Definition
	Min	Max	Min	Max	
Static Total Compressive	667 (N)	1068 (N)	150 (lbf)	240 (lbf)	The total load applied by enabling mechanism and heat sink onto the socket as transferred through the package, contacts and socket seating plane.
Dynamic Compressive	NA	588 (N)	NA	132 (lbf)	Quasi-static equivalent compressive load applied during the mechanical shock from heatsink, calculated using a reference 600g heatsink with a 25G shock input and an amplification factor of 3 (600g x 25G x 3 =441N=99 lbf). This specification can have flexibility in specific values, but the ultimate product of mass times acceleration should not exceed this value. Intel reference system shock requirement for this product family is 25G input as measured at the chassis mounting location.
Board Transient Bend Strain	NA	500 (ue) for 62 (mil); 400 (ue) for 100 (mil)	NA	500 (ue) for 62 (mil); 400 (ue) for 100 (mil)	This is the strain on boards near to socket BGA corners during transient loading events through manufacturing flow or testing. The test guidance can be found in Board Flexure Initiative (BFI) strain guidance from your local CQE.

2.4 Socket Electrical Requirements

LGA2011-3 socket electrical requirements are measured from the socket-seating plane of the processor to the component side of the socket PCB to which it is attached. All specifications are maximum values (unless otherwise stated) for a single socket contact, but include effects of adjacent contacts where indicated.

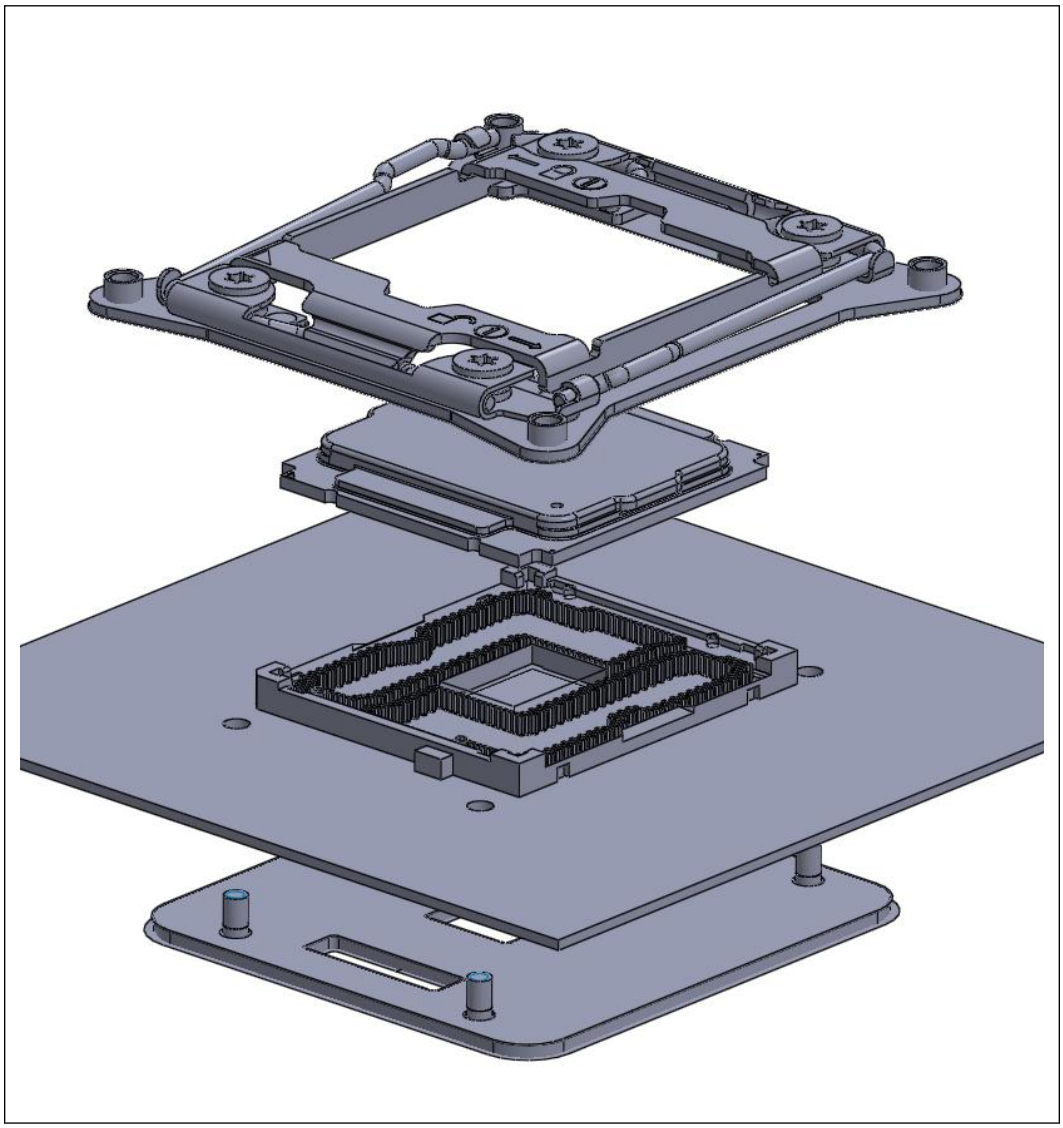
Table 4. LGA 2011-3 Socket Electrical Requirements

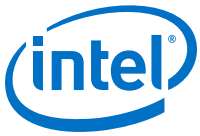
Parameter	Value	Comment
Maximum Socket Part Average Resistance (EOL @ 100°C)	25 milli-ohm	This is the maximum allowable part average socket resistance allowed under all use conditions (EOL and 100°C). This is monitored by measuring the daisy chain resistance of all socket contacts in series across the socket and dividing by the number of contacts measured. The resulting value must be below 25 milli-ohm at all use conditions (EOL) and elevated temperature (100°C).
Maximum Single Pin Resistance (mean + 4 sigma) (EOL @ 100°C)	38 milli-ohm	This is the maximum validated single contact resistance on the socket under all use conditions (EOL) and at elevated temperature (100°C). This accounts for resistance variation across the socket. While it is possible that a single contact may reach a resistance of 38 milli-ohm, the maximum socket part average resistance spec insures that all contacts averaged together will not be higher than 25 milli-ohm.
Dielectric Withstand Voltage	360 volts RMS	
Insulation Resistance	800 milli-ohm	

3.0 Independent Loading Mechanism (ILM) Specifications

The Independent Loading Mechanism (ILM) provides the force needed to seat the land LGA package onto the socket contacts. See image below for total processor stack consisting of all relevant mechanical components.

Figure 9. Processor Stack





The ILM is physically separate from the socket body. The assembly of the ILM is expected to occur after attaching the socket to the board. The exact assembly location is dependent on manufacturing preference and test flow.

The mechanical design of the ILM is a key contributor to the overall functionality of the socket. Intel performs detailed studies on integration of processor package, socket and ILM as a system. These studies directly impact the design of the ILM. The Intel reference ILM will be "built to print" from Intel controlled drawings. Intel recommends using the Intel Reference ILM. Custom non-Intel ILM designs do not benefit from Intel's detailed studies and may not incorporate critical design parameters.

The ILM has two critical functions: evenly deliver and distribute the force to seat the processor onto the socket contacts and ultimately through the socket solder joints. Another purpose of ILM is to ensure electrical integrity/performance of the socket and package.

3.1 ILM Load Specifications

The Independent Loading Mechanism (ILM) provides the force needed to seat the package onto the socket contacts.

Maximum Allowable Loads

The table below provides load specifications for the processor package. These maximum limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Exceeding these limits during test may result in component failure or other damage to the system. The processor substrate should not be used as a mechanical reference or load bearing surface for thermal solutions.

Table 5. LGA 2011-3 Maximum Allowable Loads

Item	Maximum
Static Pre-Load Compressive (ILM load)	712N (160 lbf)
Static Pre-Load Compressive (HS load)	400N (90 lbf)
Total Socket Static Compressive (ILM+HS=Socket)	1068N (240 lbf)

Minimum Allowable Loads

The ILM is designed to achieve the minimum Socket Static Pre-Load Compressive load specification. The thermal solution (heatsink) should apply additional load. The combination of an ILM and HS will be used to achieve the load targets shown in the table below.

Table 6. LGA 2011-3 Minimum Allowable Loads

Item	Minimum
Static Pre-Load Compressive (ILM load)	445N (100 lbf)
Static Pre-Load Compressive (HS load)	222N (50 lbf)
Total Socket Static Compressive (ILM+HS=Socket)	667N (150 lbf)

End of Life Load Targets

The ILM is designed to achieve the minimum end of life loads for the socket. The thermal solution (heatsink) should apply a portion of the end of life load. The combination of an ILM and HS will be used to achieve the load targets shown in the table below.

Table 7. LGA 2011-3 Minimum End of Life Loads

Item	End of Life Minimum
Static Pre-Load Compressive (ILM load)	311N (70 lbf)
Static Pre-Load Compressive (HS load)	178N (40 lbf)
Total Socket Static Compressive (ILM+HS=Socket)	490N (110 lbf)

3.2 ILM Keepout Zones (KOZ)

The table below lists envelope dimensions for ILM KOZ , both topside and backplate. For detailed views, refer to dimensioned drawings in the Mechanical Drawings section .

Table 8. LGA 2011-3 ILM General Keepout Dimensions

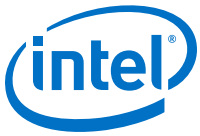
Keepout Type	ILM
Topside envelope	93x93 mm (3.6x3.7in)
ILM Hole Location	46x69.2 mm (1.8x2.7 in)
Backplate Envelope	78x84 mm (3.1x3.3 in)

3.3 Independent Loading Mechanism (ILM)

The Independent Loading Mechanism (ILM) provides the force needed to seat the package onto the socket contacts. The ILM is a mechanical assembly that is physically separate from the socket body. The assembly of the ILM to the motherboard is expected to occur after attaching the socket to the board. The exact assembly location is dependent on manufacturing preference and test flow.

The mechanical design of the ILM is a key contributor to the overall functionality of the socket. Intel performs detailed studies on integration of processor package, socket and ILM as a system. These studies directly impact the design of the ILM. The Intel reference ILM will be "built to print" from Intel controlled drawings. Intel recommends using the Intel Reference ILM. Custom non-Intel ILM designs do not benefit from Intel's detailed studies and may not incorporate critical design parameters.

The ILM has two critical functions: deliver the force to seat the processor onto the socket contacts resulting in even load transfer through the socket solder joints. Another purpose of ILM is to ensure electrical integrity/performance of the socket and package.



3.4 ILM Mechanical Design Considerations and Recommendations

An retention/loading mechanism must be designed to support the processor heatsink and to ensure processor interface with the socket contact is maintained since there are no features on the socket for direct attachment of the heatsink or retaining the processor. In addition to supporting the processor heatsink over the processor, this mechanism plays a significant role in the robustness of the system in which it is implemented, in particular:

- Ensuring that thermal performance of the TIM applied between the IHS and the heatsink is achievable. TIMs, especially those based on phase change materials, are very sensitive to applied pressure: the higher the pressure, the better the initial performance. TIMs such as thermal greases are not as sensitive to applied pressure. Designs should consider the impact of shock and vibration events on TIM performance as well as possible decrease in applied pressure over time due to potential structural relaxation in enabled components.
- Ensuring that system electrical, thermal, and structural integrity is maintained under shock and vibration events. The mechanical requirements of the attach mechanism depend on the weight of the heatsink, as well as the level of shock and vibration that the system must support. The overall structural design of the baseboard and system must be considered when designing the heatsink and ILM attach mechanism. Their design should provide a means for protecting the socket solder joints as well as preventing package pullout from the socket.
- The load applied by the attachment mechanism and the heatsink must comply with the package specifications, along with the dynamic load added by the mechanical shock and vibration requirements of the package and socket.
- Load induced onto the package and socket by the ILM may be influenced with heatsink installed. Determining the performance for any thermal/mechanical solution is the responsibility of the customer.

A potential mechanical solution for heavy heatsink is the use of a supporting mechanism such as a backer plate or the utilization of a direct attachment of the heatsink to the chassis pan. In these cases, the strength of the supporting component can be utilized rather than solely relying on the baseboard strength. In addition to the general guidelines given above, contact with the baseboard surfaces should be minimized during installation in order to avoid any damage to the baseboard.

Placement of board-to-chassis mounting holes also impacts board deflection and resultant socket solder ball stress. Customers need to assess the shock for their designs as heatsink retention (back plate), heatsink mass and chassis mounting holes may vary.

3.5 ILM Features

The ILM is defined by four basic features

1. ILM Loadplate: Formed sheet metal that when closed applies four point loads onto the IHS seating the processor into the socket
2. ILM Frame: Single piece or assembly that mounts to PCB board and provides the hinge locations for the levers the ILM frame also contains captive mounts for heatsink attach. An insulator is pre applied by the vendor to the bottom side of the ILM frame.

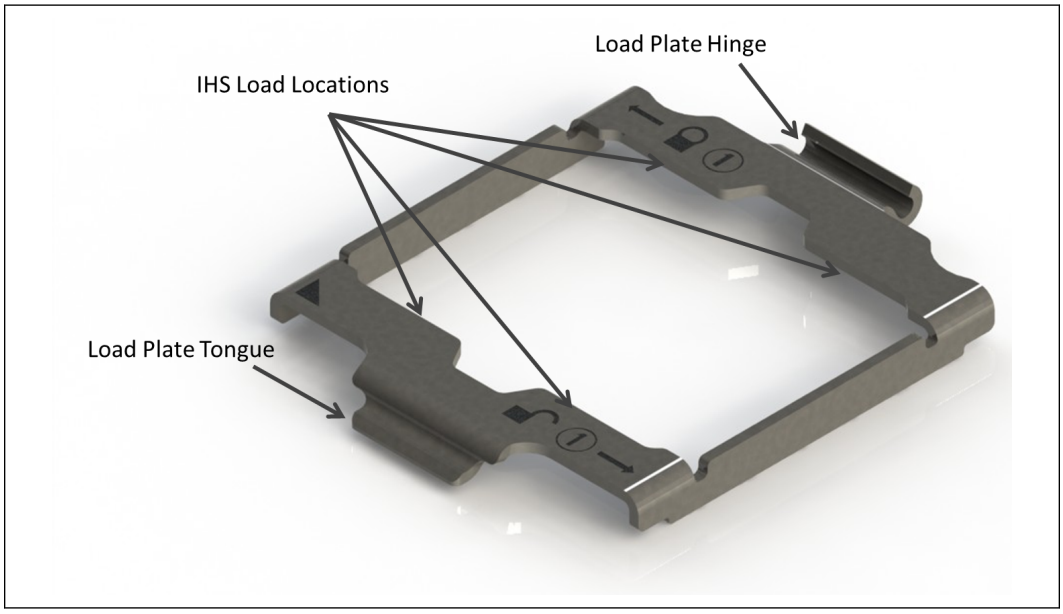
3. ILM Actuation levers: Formed loading levers designed to place equal force on both ends of the ILM load plate. Some of the load is passed through the socket body to the board inducing a slight compression on the solder joints
4. ILM Backplate: A flat steel back plate with threaded studs to attach to the ILM frame. A clearance hole is located at the center of the plate to allow access to test points and backside capacitors. Two additional cut-outs on the backplate provide clearance for backside voltage regulator components. An insulator is pre applied by the vendor to the side with the threaded studs.

Heatsink mounting studs on ILM frame allow for topside thermal solution attach to a rigid structure. This eliminates the motherboard thickness dependency from the heatsink mechanical stackup. ILM assembly provides a clamping force between the ILM frame, backplate and board, resulting in reduced board bending leading to higher solder joint reliability. ILM lever design provides an interlocking mechanism to ensure proper opening or closing sequence for the operator.

ILM Load Plate Design

Four point loading contributes to minimizing package and socket warpage under non uniformly distributed load. The reaction force from closing the load plate is transmitted to the frame and through the captive fasteners to the back plate. Some of the load is passed through the socket body to the board inducing a slight compression on the solder joints.

Figure 10. ILM Load Plate



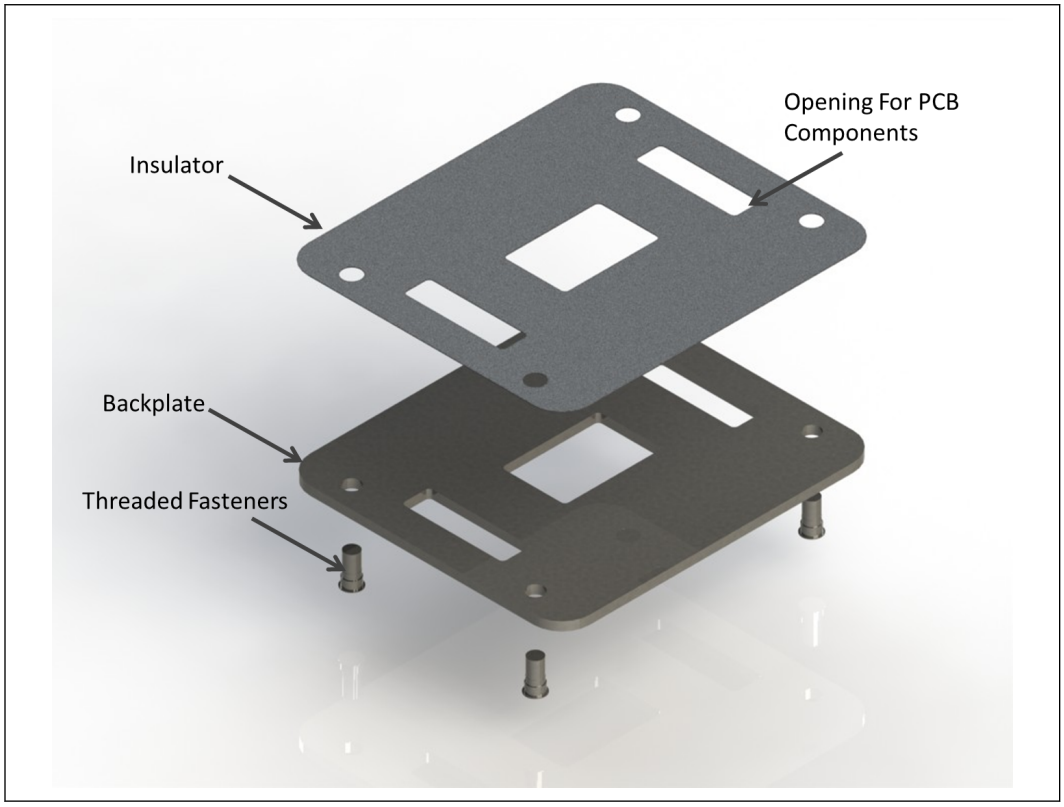
Lever Actuation/Release Forces

Maximum allowable force to actuate the levers not to exceed 4.7 lbf (21 N) at the point of typical finger placement.

ILM Back Plate Design

The backplate assembly consists of a supporting plate and captive standoffs. It provides rigidity to the system to ensure minimal board and socket deflection. Four externally threaded (male) inserts which are press fit into the back plate are for ILM attachment. Three cavities are located at the center of the plate to allow access to the baseboard test points and backside capacitors. An insulator is pre-applied to prevent shorting the board.

Figure 11. ILM Backplate

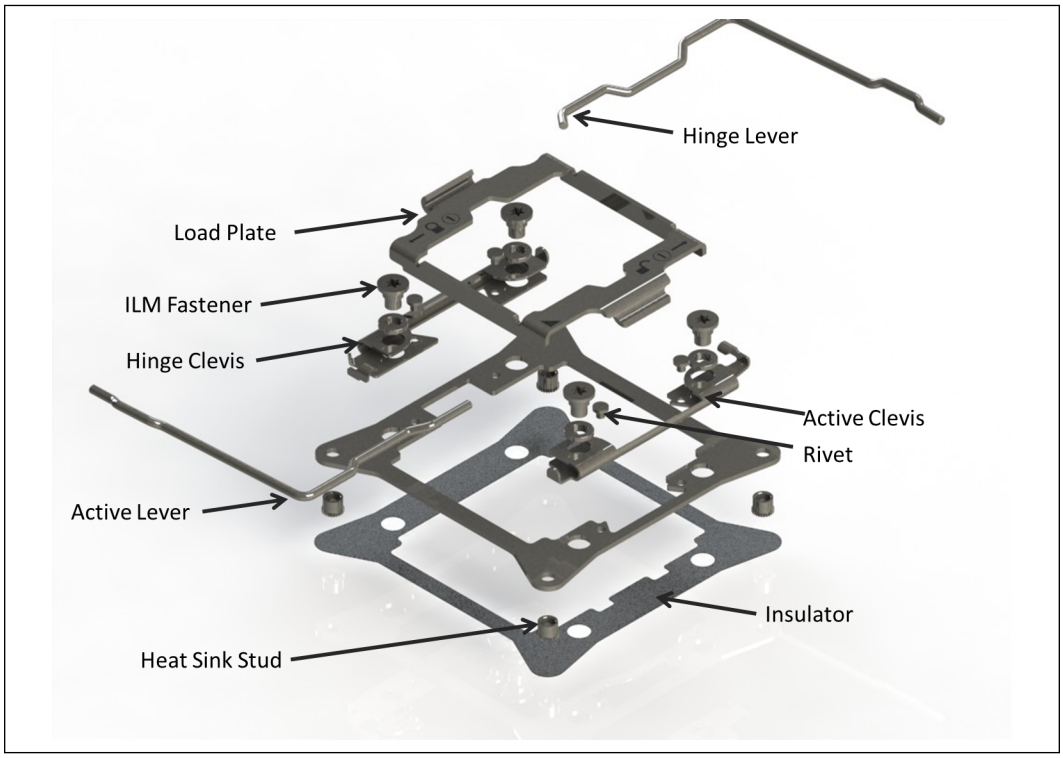


3.6 Intel® ILM Reference Designs

3.6.1 ILM

The ILM consists of two sub assemblies that will be procured as a set from the enabled vendors. These two components are the ILM assembly and back plate. The ILM assembly consists of several pieces as shown and labeled in the following diagram. The hinge lever, active lever, load plate, top plate,clevises, and the captive fasteners. For clarity the ILM cover is not shown in this view.

Figure 12. Exploded ILM



An assembled view is shown in the following figure.

Figure 13. Assembled ILM

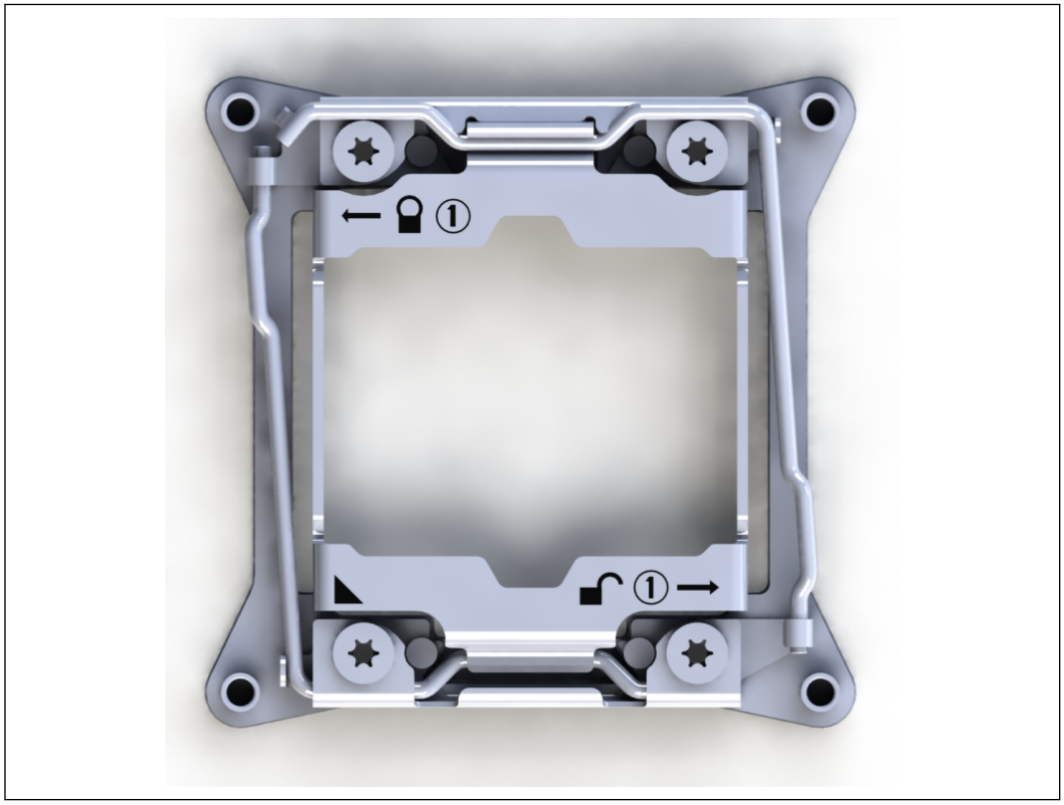


Table 9. ILM Component Thickness and materials

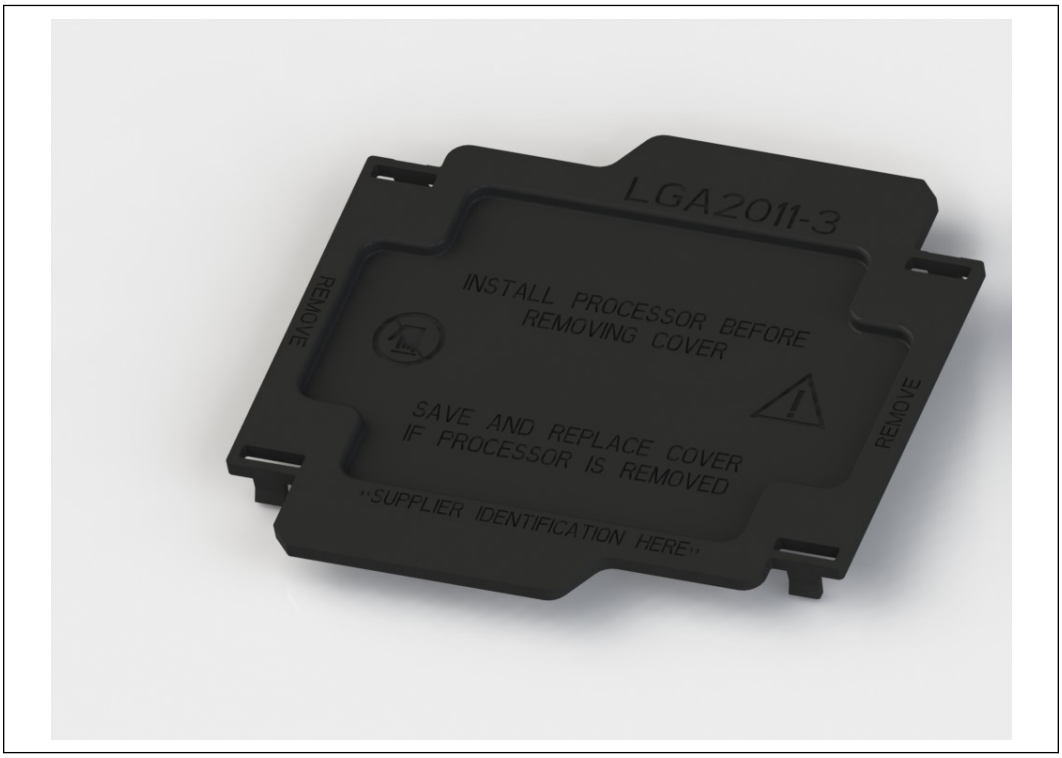
Component	Thickness	Material
ILM Frame	1.20 mm	310 Stainless Steel
ILM Load Plate	1.50 mm	310 Stainless Steel
ILM Back Plate	2.20 mm	S50C low Carbon Steel

3.7 ILM Cover

Intel has developed a cover that will snap on to the ILM for the LGA2011 socket family.

The ILM cover is intended to reduce the potential for socket contact damage from the operator / customer fingers being close to the socket contacts to remove or install the pick and place cover. By design the ILM cover and pick and place covers can not be installed simultaneously. This cover is intended to be used in place of the pick and place cover once the ILM is assembled to the board. The ILM will be offered with the ILM cover pre assembled as well as a discrete part.

Figure 14. ILM cover



- Pre-assembled by the ILM vendors to the ILM load plate. It will also be offered as a discrete component.
- The ILM cover will pop off if a processor is installed in the socket.
- Maintain inter-changeability between validated ILM vendors for LGA2011-3 socket.
- The ILM cover for the LGA2011-3 socket will have a flammability rating of V-0 per UL 60950-1.

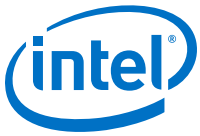
Note: Intel recommends removing the Pick and Place cover (PnP) of the socket body in manufacturing as soon as possible at the time when ILM is being installed.

ILM Cover Attach/Removal Force

The required force to remove the ILM cover shall not exceed 7.6 N when the load is applied by finger at the center of cover.

3.8 ILM Allowable Board Thickness

The ILM components described in this document will support board thickness in the range of 1.5748 - 2.54 mm (0.062" - 0.100"). Boards (PCBs) not within this range may require modifications to the back plate or other ILM components retention. Contact the component suppliers (Component Suppliers on page 50) for modifications.



4.0 Processor Thermal Specifications and Features

4.1 T_{case} and DTS-Based Thermal Specification Implementation

Thermal solutions should be sized such that the processor complies to the T_{CASE} thermal profile all the way up to TDP, because, when all cores are active, a thermal solution sized as such will have the capacity to meet the DTS thermal profile, by design. When all cores are not active or when Intel Turbo Boost Technology is active, attempting to comply with the DTS thermal profile may drive system fans to speeds higher than the fan speed required to comply with the T_{CASE} thermal profile at TDP.

In cases where thermal solutions are undersized, and the processor does not comply with the T_{CASE} thermal profile at TDP, compliance can occur when the processor power is kept lower than TDP, **AND** the actual T_{CASE} is below the T_{CASE} thermal profile at that lower power.

In most situations, implementation of DTS thermal profile can reduce average fan power and improve acoustics, as compared to $T_{CONTROL}$-based fan speed control.

4.1.1 Margin to Thermal Specification (M)

To simplify processor thermal specification compliance, the processor calculates and reports margin to DTS thermal profile (M) using the following method.

Processor reads firmware programmable values:

1. TCC_OFFSET: In-band: TEMPERATURE_TARGET[27:24]

Note: TCONTROL_OFFSET for the Intel® Core™ i7 Processor Family for the LGA2011-3 Socket is zero (0).

Processor gathers information about itself:

1. Processor stores the intercept and slope terms (T_{LA} and Ψ_{PA}) from the DTS Thermal Profile for that particular SKU (one-time read only)
2. Processor reads its own energy consumption and calculates power, P
3. Processor reads its own temperature, DTS

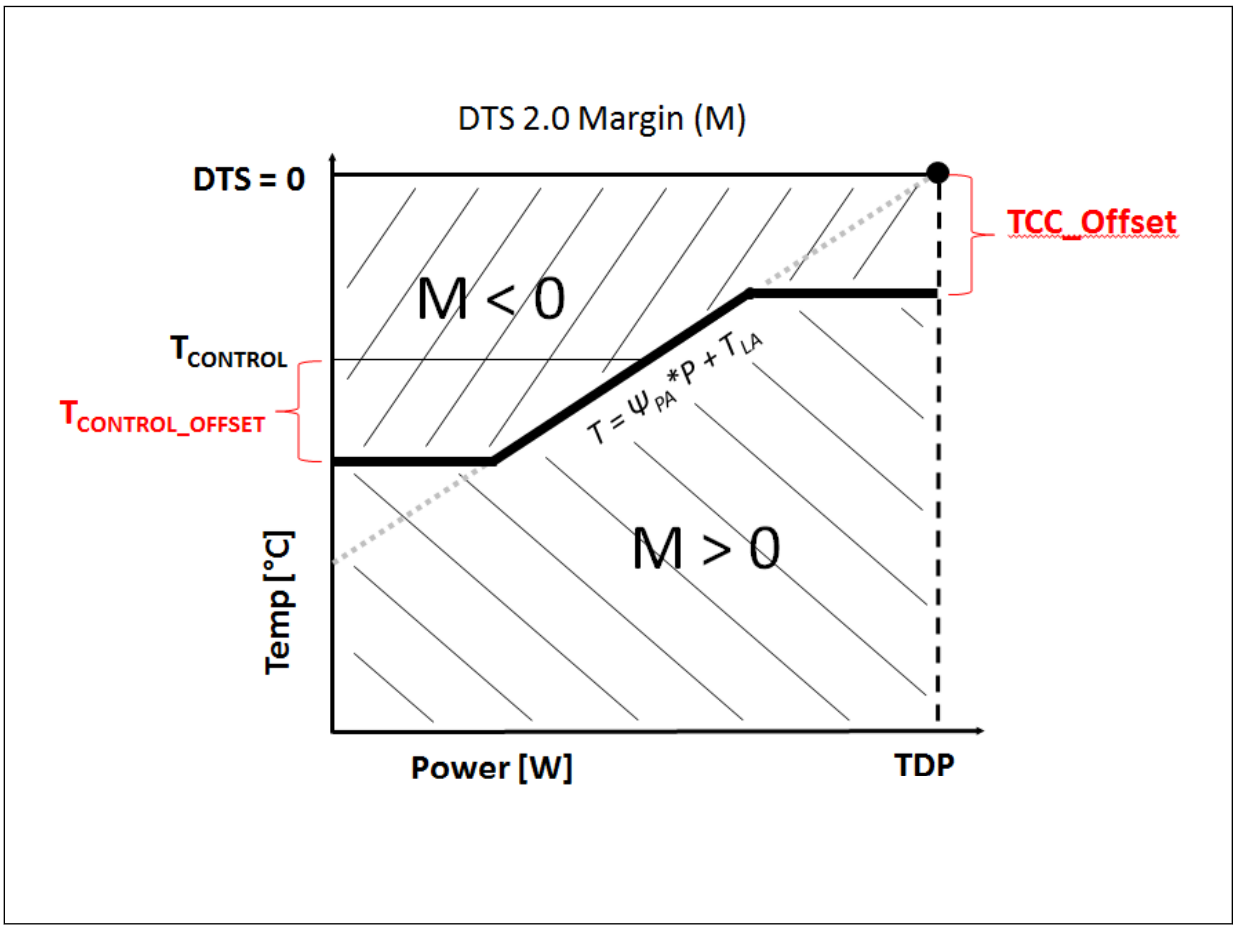
Finally, processor calculates the margin value (M) to the specification (solid black line in the graph below). The PECI command for reading margin (M) is RdPkgConfig(), Index 10.

M < 0 indicates gap to spec, processor needs more cooling (for example, increase fan speed)

M > 0 this indicates margin to spec, processor is sufficiently cooled

Graphically, this is represented below (firmware programmable values shown in red)

Figure 15. Margin to Thermal Spec (M)



DTS 2.0 processor margin values can be obtained via PECI or processor registers. Refer to the Processor Datasheet Volume 2 (see Reference Documents).

Table 10. DTS 2.0 Margin From PECI

Service	Index Value (IV) (decimal)	Parameter Value (word)	RdPkgConfig() Data (dword)	WrPkgConfig() Data (dword)	Description
Thermal Margin	10	0x0000	15:0--Package Temperature margin in 8.8 format, 32:16--Reserved	N/A	Package temperature margin with regards to DTS Thermal Profile. Positive indicates thermal margin, and package is less than DTS thermal profile

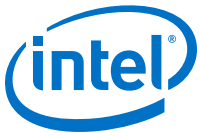


Table 11. DTS 2.0 Margin From Processor Register: CSR for PACKAGE_THERM_MARGIN

Bus:1		Device:30	Function:0 Offset:E0
Bit	**Attr**	**Default**	**Description**
31:16	RSVD-P	0000h	Reserved--Protected
15:0	R0-V	0000h	THERM_MARGIN--This field provides Platform Firmware with running average of the instantaneous temperature margin above Tspec in 2's complement 8.8 format. This is the recommended field for Platform firmware to use for fan control. When this value is negative, it indicates a firmware must increase the fan speed. With a positive value, firmware may decrease the speed of the fan
Note: • DTS 2.0 Thermal Margin CSR is a mirror of MSR (1A1h) PACKAGE_THERM_MARGIN			

4.2 Processor Thermal Features

4.2.1 Adaptive Thermal Monitor

The Adaptive Thermal Monitor feature provides an enhanced method for controlling the processor temperature when the processor silicon reaches its maximum operating temperature. Adaptive Thermal Monitor uses Thermal Control Circuit (TCC) activation to reduce processor power via a combination of methods. The first method, Frequency Control, involves the processor reducing its operating frequency. The second method, Clock Modulation, reduces power consumption by modulating (starting and stopping) the internal processor core clocks. The processor intelligently selects the appropriate method on a dynamic basis. BIOS is not required to select a specific method. The Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it is immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and in some cases may exceed the specified maximum temperature which affects the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously. Refer to the Processor Thermal Solutions on page 35 for information on designing a compliant thermal solution.

The Adaptive Thermal Monitor feature must be enabled for the processor to be operating within specifications. Snooping and interrupt processing are performed in the normal manner while the TCC is active.

Frequency Control

The Adaptive Thermal Monitor uses frequency control to lower its operating frequency. Reducing the processor frequency reduces the processor power consumption. The first operating point represents the normal operating condition for the processor. The remaining points consist of lower operating frequencies. When the TCC is activated,

the processor automatically transitions to the new lower operating frequency. This transition occurs on the order of microseconds, µs. The processor continues to execute instructions during this frequency transition.

Clock Modulation

Clock modulation is performed by alternately turning the clocks off and on at a duty cycle specific to the processor. The period of the duty cycle is configured to 32 microseconds when the TCC is active. Cycle times are independent of processor frequency. Clock modulation may also be initiated by software at a configurable duty cycle.

With either method, a small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor is near its maximum operating temperature. Once it has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive.

4.2.2 On-Demand Mode

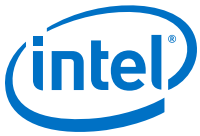
The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as "On-Demand" mode and is distinct from the Adaptive Thermal Monitor feature. On-Demand mode is intended as a means to reduce system power consumption. Systems should not rely on software usage of this mechanism to limit the processor temperature. If bit 4 of the IA32_CLOCK_MODULATION MSR is set to a '1', the processor will immediately reduce its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:0 of the same IA32_CLOCK_MODULATION MSR. In On-Demand mode, the duty cycle can be programmed from 6.25% on / 93.75% off to 93.75% on / 6.25% off in 6.25% increments. On-Demand mode may be used in conjunction with the Adaptive Thermal Monitor; however, if the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

4.2.3 PROCHOT_N Signal

For a detailed description of the PROCHOT_N Signal see *Haswell-EN/EP/EP 4S/EX Processor External Design Specification (EDS), Volume One: Architecture*.

4.2.4 THERMTRIP_N Signal

Regardless whether Adaptive Thermal Monitor is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when the processor has reached an elevated temperature. At this point, the THERMTRIP_N signal will go active and stay active. THERMTRIP_N activation is independent of processor activity and does not generate any Intel® QuickPath Interconnect transactions. If THERMTRIP_N is asserted, all processor power rails must be removed within a certain amount of time. Refer to the Processor Datasheet, Volume 1 (see Reference Documents) for timing specifications for removing power rails. The temperature at which THERMTRIP_N asserts is not user configurable and is not software visible.



4.2.5 Absolute Processor Temperature

The processor has a software readable field in the TEMPERATURE_TARGET register that contains the minimum temperature at which the Thermal Control Circuit (TCC) will be activated and PROCHOT_N will be asserted.

Intel does not test any third party software that reports absolute processor temperature. As such, Intel cannot recommend the use of software that claims this capability. Since there is part-to-part variation in the TCC (thermal control circuit) activation temperature, use of software that reports absolute temperature could be misleading.

4.3 Processor Thermal Specifications

The processor requires a thermal solution to maintain temperatures within operating limits. Any attempt to operate the processor outside these limits may result in permanent damage to the processor and potentially other components within the system. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor integrated heat spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.

For more information on designing a component level thermal solution, refer to Processor Thermal Solutions on page 35.

4.3.1 Thermal Specifications

To allow optimal operation and long-term reliability of Intel processor-based systems, the processor must remain between the minimum and maximum case temperature (T_{CASE}) specifications as defined in the tables in the following sub-sections. Thermal solutions that do not provide sufficient thermal cooling may affect the long-term reliability of the processor and system.

Thermal profiles ensure adherence to Intel reliability requirements.

Intel assumes specific system boundary conditions (system ambient, airflow, heatsink performance / pressure drop, preheat, etc.) for each processor SKU to develop T_{case} and DTS thermal specifications. For servers each processor will be aligned to wither 1U or 2U system boundary conditions. Customers can use other boundary conditions (for example a better thermal solution with higher ambient) providing they are compliant to those specifications. Furthermore, implementing a thermal solution that violates the thermal profile for extended periods of time may result in permanent damage to the processor or reduced life. The upper point of the thermal profile consists of the Thermal Design Power (TDP) and the corresponding T_{CASE_MAX} value (x = TDP and y = T_{CASE_MAX}) represents a thermal solution design point.

Intel recommends that thermal solution designs target the Thermal Design Power (TDP). The Adaptive Thermal Monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. The Adaptive Thermal Monitor feature must be enabled for the processor to remain within its specifications.

4.3.2 T_{CASE} and DTS Based Thermal Specifications

To simplify compliance to thermal specifications at processor run time, the processor has a Digital Thermal Sensor (DTS) based thermal specification. Digital Thermal Sensor outputs a relative die temperature from TCC activation temperature. T_{CASE}-based specifications are used for heatsink sizing while DTS-based specs are used for acoustic and fan speed optimizations while the server is operating. Some SKUs may share the same T_{CASE} thermal profiles but have distinct DTS thermal profiles.

All thermal profiles, whether based on T_{CASE} or DTS, follow the straight-line equation format namely, $y = mx + b$. Where,

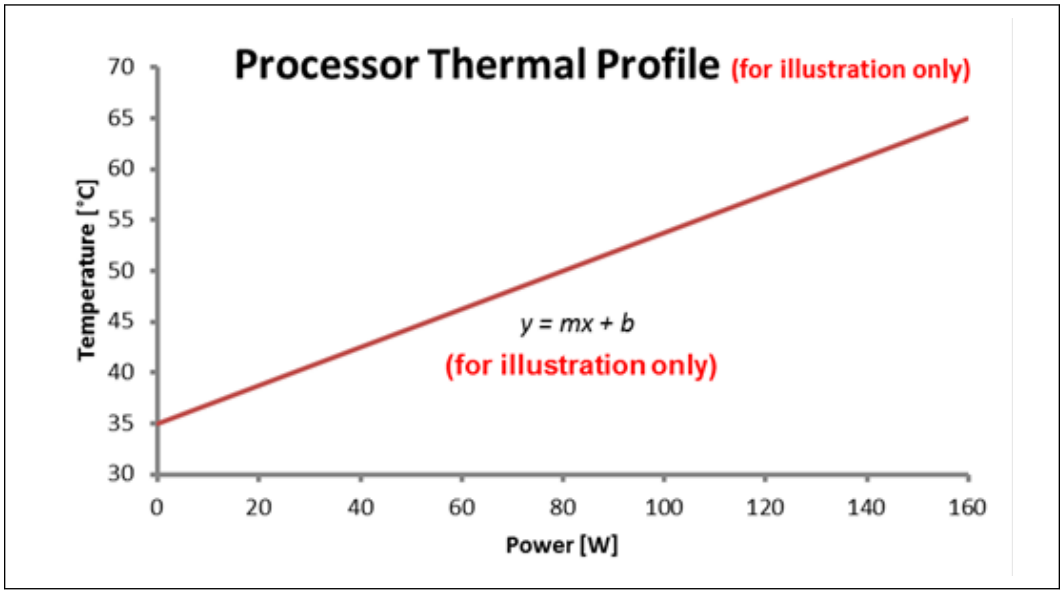
y = temperature (T) in °C

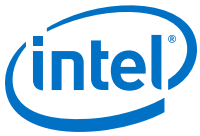
m = slope (Ψ)

x = power (P) in Watts

b = y-intercept (T_{LA}) (LA = local ambient)

Figure 16. Typical Thermal Profile Graph (Illustration Only)





4.3.3 Processor Thermal Specifications

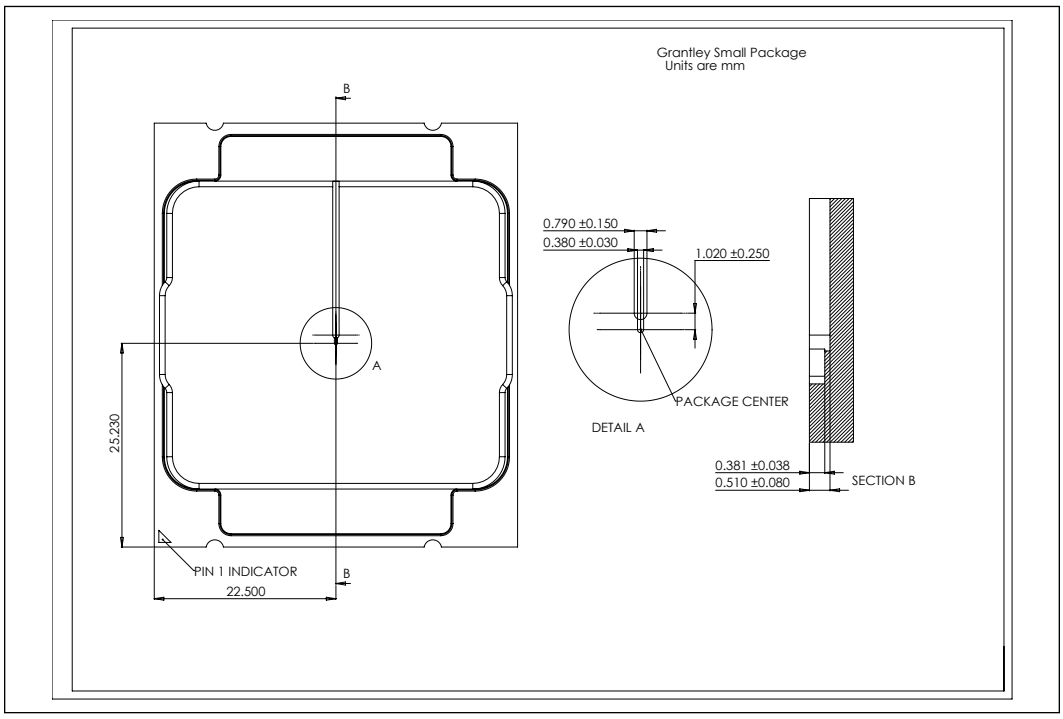
Processor Number	TDP (W) [2]	Core Count	$T_{CONTROL}$	Thermal Profiles [6]		Notes
				T_{CASE} [5]	DTS	
i7-5960X	140	8	18	T_C=[0.170*P] + 43.3	T_{DTS}=[0.398*P] + 43.3	1, 3, 4
i7-5930K	140	6	10	T_C=[0.170*P] + 43.2	T_{DTS}=[0.396*P] + 43.2	1, 3, 4
i7-5820K	140	6	10	T_C=[0.170*P] + 43.2	T_{DTS}=[0.396*P] + 43.2	1, 3, 4

Notes:
1. These values are specified at VccIN_MAX for all processor frequencies. Systems must be designed to ensure the processor is not subjected to any static Vcc and Icc combination wherein VccIN exceed VccIN_MAX at a specified Icc. Refer to the electrical loadline specifications.
2. Thermal Design Power (TDP) should be used as a target for processor thermal solution design at maximum T_{CASE}. Processor power may exceed TDP for short durations. See Intel Turbo Boost Technology.
3. These specifications are based on initial pre-silicon simulations and are subject to change as further characterization data becomes available.
4. Power specifications are defined at all VIDs found in the Processor Datasheet, Volume 1 (see Reference Documents).
5. The T_{CASE} Thermal Profile is based on the LGA2011-0 Thermal Test Vehicle (TTV).
6. Ψ_{PA} specifications are based on the DRA-A and T-HPHS thermal solutions. Therefore, there is no change to the requirements from the 2nd and 3rd Generation Intel® Core™ i7 processors for the LGA2011 socket.

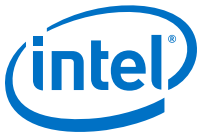
4.3.4 Thermal Metrology

The minimum and maximum case temperatures (T_{CASE}) specified are measured at the geometric top center of the processor integrated heat spreader (IHS). The following figures illustrate the location where T_{CASE} temperature measurements should be made. The figures also include geometry guidance for modifying the IHS to accept a thermocouple probe.

Figure 17. Case Temperature (T_{CASE}) Measurement Location



Note: Figure is not to scale and is for reference only.



5.0 Processor Thermal Solutions

5.1 Heatsink Design Considerations

To remove the heat from the processor, three basic parameters should be considered:

- The area of the surface on which the heat transfer takes place - Without any enhancements, this is the surface of the processor package IHS. One method used to improve thermal performance is to attach a heatsink to the IHS. A heatsink can increase the effective heat transfer surface area by conducting heat out of the IHS and into the surrounding air through fins attached to the heatsink base.
- The conduction path from the heat source to the heatsink fins - Providing a direct conduction path from the heat source to the heatsink fins and selecting materials with higher thermal conductivity typically improves heatsink performance. The length, thickness, and conductivity of the conduction path from the heat source to the fins directly impact the thermal performance of the heatsink. In particular, the quality of the contact between the package IHS and the heatsink base has a higher impact on the overall thermal solution performance as processor cooling requirements become strict. Thermal interface material (TIM) is used to fill in the gap between the IHS and the bottom surface of the heatsink, and thereby improves the overall performance of the thermal stackup (IHS-TIM-Heatsink). With extremely poor heatsink interface flatness or roughness, TIM may not adequately fill the gap. The TIM thermal performance depends on its thermal conductivity as well as the pressure load applied to it.
- The heat transfer conditions on the surface upon which heat transfer takes place - Convective heat transfer occurs between the airflow and the surface exposed to the flow. It is characterized by the local ambient temperature of the air, TLA, and the local air velocity over the surface. The higher the air velocity over the surface, the more efficient the resulting cooling. The nature of the airflow can also enhance heat transfer via convection. Turbulent flow can provide improvement over laminar flow. In the case of a heatsink, the surface exposed to the flow includes the fin faces and the heatsink base.

An active heatsink typically incorporates a fan that helps manage the airflow through the heatsink.

Passive heatsink solutions require in-depth knowledge of the airflow in the chassis. Typically, passive heatsinks see slower air speed. Therefore, these heatsinks are typically larger (and heavier) than active heatsinks due to the increase in fin surface necessary to meet a required performance. As the heatsink fin density (the number of fins in a given cross-section) increases, the resistance to the airflow increases; it is more likely that the air will travel around the heatsink instead of through it, unless air bypass is carefully managed. Using air-ducting techniques to manage bypass area is an effective method for maximizing airflow through the heatsink fins.

5.2 Thermal Design Guidelines

5.2.1 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is a feature available on certain Intel® Core™ i7 Processor Family for the LGA2011-3 Socket SKUs that opportunistically, and automatically allows the processor to run faster than the marked frequency if the part is operating below certain power and temperature limits. With Turbo Boost enabled, the instantaneous processor power *can exceed TDP for short durations* resulting in increased performance.

System thermal design should consider the following important parameters (set via BIOS):

- POWER_LIMIT_1 (PL1) = average processor power over a long time window (default setting is TDP)
- POWER_LIMIT_2 (PL2) = average processor power over a short time window above TDP (short excursions). Maximum allowed by the processor is 20% above TDP for all SKUs (1.2 * TDP). Note that actual power will include IMON inaccuracy.
- POWER_LIMIT_1_TIME (Tau) = time constant for the exponential weighted moving average (EWMA) which optimizes performance while reducing thermal risk. (dictates how quickly power decays from its peak)

Please note that although the processor can exceed PL1 (default TDP) for a certain amount of time, the *exponential weighted moving average (EWMA) power will never exceed PL1*.

A properly designed processor thermal solution is important to maximizing Turbo Boost performance. However, heatsink performance (thermal resistance, Ψ_{CA}) is only one of several factors that can impact the amount of benefit. Other factors are operating environment, workload and system design. With Turbo Mode enabled, the processor may run more consistently at higher power levels, and be more likely to operate above $T_{CONTROL}$, as compared to when Turbo Mode is disabled. This may result in higher acoustics.

5.2.2 Thermal Excursion Power

Under fan failure or other anomalous thermal excursions, processor temperature (either T_{CASE} or DTS) may exceed the thermal profile for a duration totaling less than 360 hours per year without affecting long term reliability (life) of the processor. For more typical thermal excursions, Thermal Monitor is expected to control the processor power level as long as conditions do not allow the processor to exceed the temperature at which Thermal Control Circuit (TCC) activation initially occurred.

Under more severe anomalous thermal excursions when the processor temperature cannot be controlled at or below thermal profile by TCC activation, then data integrity is not assured. At some higher thresholds, THERMTRIP_N will enable a shut down in an attempt to prevent permanent damage to the processor.

5.2.3 Thermal Characterization Parameters

The case-to-local ambient Thermal Characterization Parameter (Ψ_{CA}) is defined by:

$$\Psi_{CA} = (T_{case} - T_{LA}) / TDP$$

Where:

T_{CASE} = Processor case temperature (°C)

T_{LA} = Local ambient temperature before the air enters the processor heatsink (°C)

TDP = TDP (W) assumes all power dissipates through the integrated heat spreader. This inexact assumption is convenient for heatsink design.

$\Psi_{CA} = \Psi_{CS} + \Psi_{SA}$

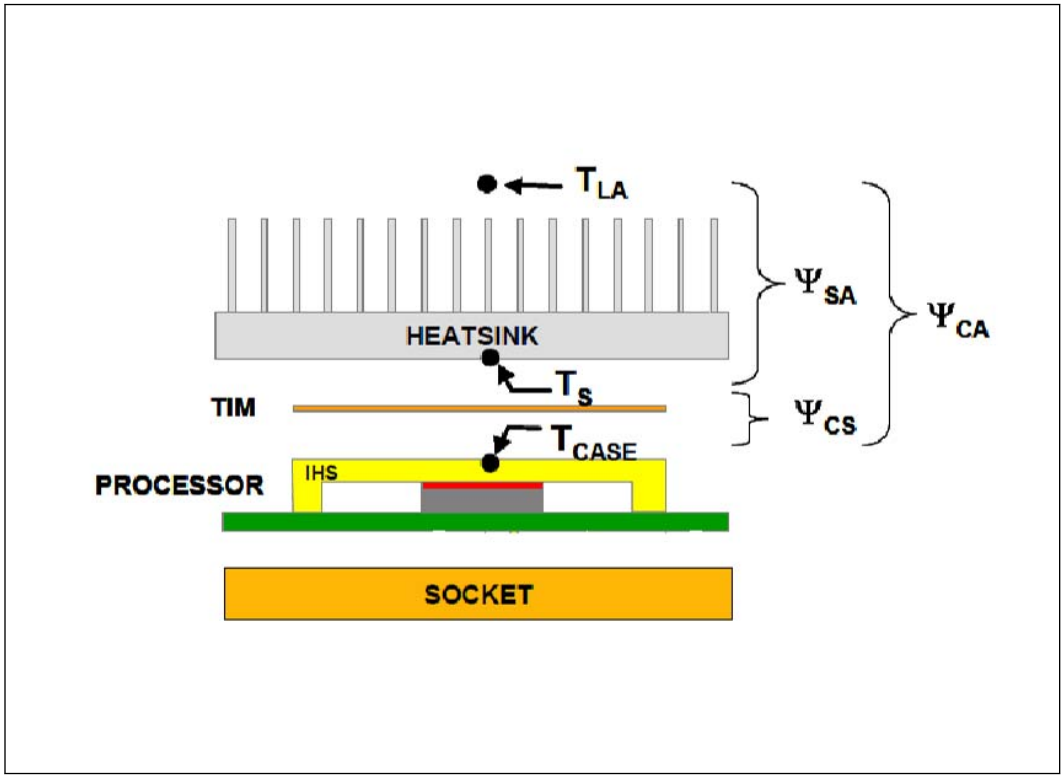
Where:

Ψ_{CS} = Thermal characterization parameter of the TIM (°C/W) is dependent on the thermal conductivity and thickness of the TIM.

Ψ_{SA} = Thermal characterization parameter from heatsink-to-local ambient (°C/W) is dependent on the thermal conductivity and geometry of the heatsink and dependent on the air velocity through the heatsink fins.

The following figure illustrates the thermal characterization parameters.

Figure 18. Thermal Characterization Parameters



5.3 Thermal Interface Material (TIM) Considerations

Thermal Interface Material between the processor IHS and the heatsink base is necessary to improve thermal conduction from the IHS to the heatsink. Many thermal interface materials can be pre-applied to the heatsink base prior to shipment from the heatsink supplier without the need for a separate TIM dispense or attachment process in the final assembly factory.

All thermal interface materials should be sized and positioned on the heatsink base in a way that ensures that the entire area is covered. It is important to compensate for heatsink-to-processor positional alignment when selecting the proper TIM size.

When pre-applied material is used, it is recommended to have a protective cover. Protective tape is not recommended as the TIM could be damaged during its removal step.

Thermal performance usually degrades over the life of the assembly and this degradation needs to be accounted for in the thermal performance. Degradation can be caused by shipping and handling, environmental temperature, humidity conditions, load relaxation over time, temperature cycling or material changes (most notably in the TIM) over time. For this reason, the measured T_{CASE} value of a given processor may increase over time, depending on the type of TIM material.

5.4 Mechanical Recommendations and Targets

Thermal solutions should be designed to meet the mechanical requirements described in this section.

Keep in mind that the heatsink retention will need to apply additional load in order to achieve the minimum Socket Static Total Compressive load. This load should be distributed over the IHS (Integrated Heat Spreader). The dual-loading approach is represented by the following equation.

$F_{ILM} + F_{HEATSINK} = F_{SOCKET}$

5.4.1 Processor / Socket Stackup Height

The following table provides the stackup height of a processor and LGA2011-3 socket with processor fully seated. This value is the root sum of squares summation of: (a) the height of the socket seating plane above the motherboard after reflow, (b) the height of the package, from the package seating plane to the top of the IHS, and accounting for its nominal variation and tolerances given in the processor, socket and ILM drawings

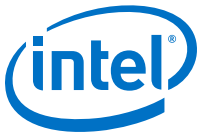
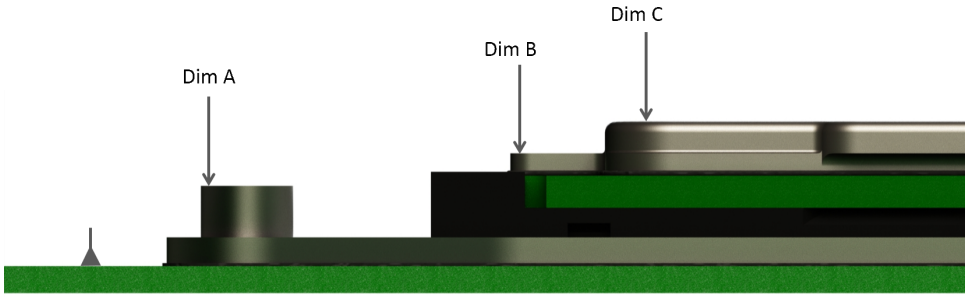


Table 12. Target Stackup Heights From Top of Board to Top of IHS

	Intel® Core™ i7 Processor Family for the LGA2011-3 Socket[1,2,4]	Platform Mid Stack Targets[1,2,3,4]
Integrated Stackup Height From Top of Board to Top of ILM Stud (Dimension A)	4.678 (+0.367)/(-0.231mm)	
Integrated Stackup Height From Top of Board to Top of IHS Load Lip (Dimension B)	6.581±0.289	6.578±0.291
Integrated Stackup Height From Top of Board to Top of IHS (Dimension C)	8.481±0.279	8.600±0.399

Notes:
1. Tolerance Stackus are a Root Sum of Squares (RSS) of all components in stack calculation using mother board surface as the reference point
2. Intel® Core™ i7 Processor Family for the LGA2011-3 Socket Stackup targets are inclusive of all package sizes (large and small)
3. Platform targets are mid stack target using minimum and maximum RSS tolerance values of all packages compatible with LGA 2011-3
4. All packages are compatible with reference retention solutions and will meet mechanical specifications

Figure 19. Integrated Stack Up Height



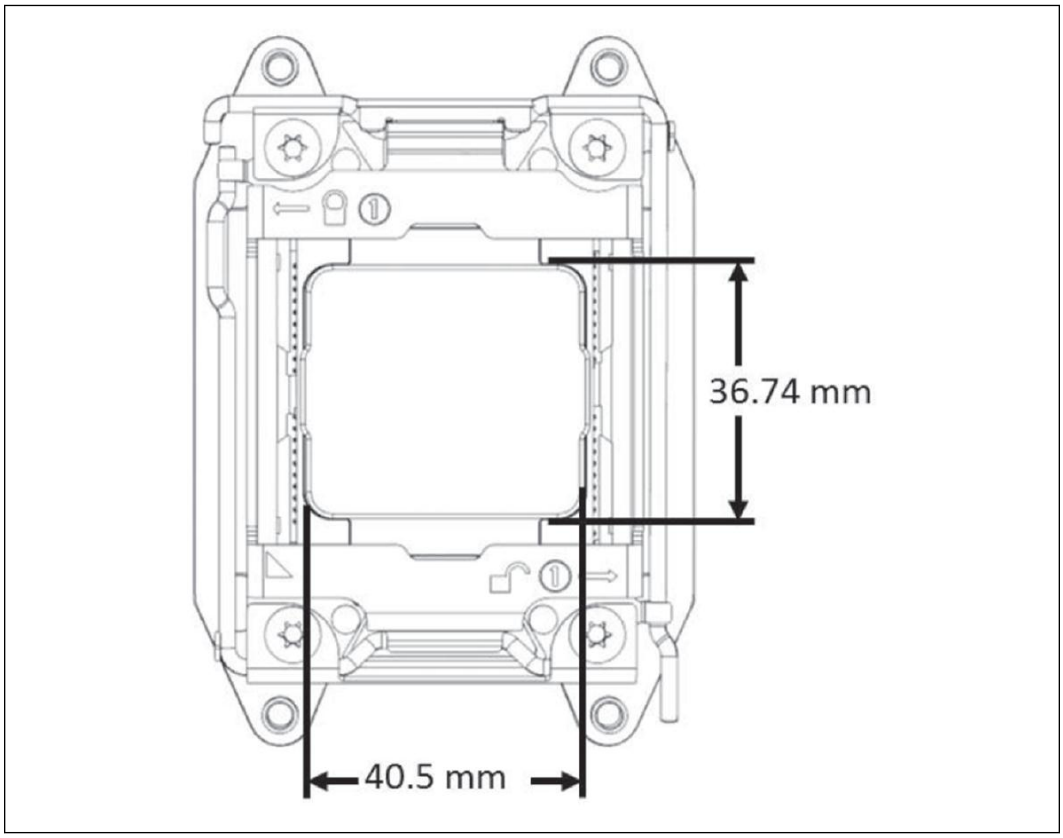
Note: ILM components removed for clarity

The table below provides the available surface dimensions for cooling the processor when fully seated in LGA2011-3 socket. This value is the X and Y dimensions for the flat top of the IHS.

Table 13. Available Cooling Area for IHS

Available Area	40.5 mm x 36.74 mm (1.594 in x 1.446 in)

Figure 20. Available Cooling Area for IHS

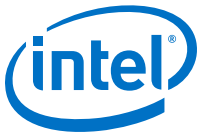


5.4.2 Processor Heatsink Mechanical Targets

Table 14. Heatsink Mechanical Targets

Parameter	Min	Max	Notes
Heatsink Mass (includes retention)		600 g (1.32 lbm)	3
Heatsink Applied Static Compressive Load	222 N (50 lbf)	400 N (90 lbf)	1,2
Heatsink Applied Dynamic only Compressive load		445 N (100 lbf)	1,4,5

Notes:
1. These specifications apply to uniform compressive loading in a direction perpendicular to the processor top surface (IHS).
2. This is the minimum and maximum static force that can be applied by the heatsink retention to the processor top surface (IHS).
3. This specification prevents excessive baseboard deflection during dynamic events.
4. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
5. An experimentally validated test condition used a heatsink mass of 1.32 lbm (600g) with 25 G acceleration measured on a shock table with a dynamic amplification factor of 3. This specification can have flexibility in specific values, but the ultimate product of mass times acceleration should not exceed this validated dynamic load (1.32 lbm x 25 G x 3= 100 lbf).



5.5 Heatsink Mechanical and Structural Considerations

An attachment mechanism must be designed to support the heatsink because there are no features on the socket on which to directly attach a heatsink. In addition to holding the heatsink in place on top of the IHS, this mechanism plays a significant role in the performance of the system, in particular:

- Ensuring thermal performance of the TIM applied between the IHS and the heatsink. TIMs, especially those based on phase change materials, are very sensitive to applied pressure: the higher the pressure, the better the initial performance. TIMs such as thermal greases are not as sensitive to applied pressure. Designs should consider the possible decrease in applied pressure over time due to potential structural relaxation in enabled components.
- Ensuring system electrical, thermal, and structural integrity under shock and vibration events, particularly the socket solder joints. The mechanical requirements of the attachment mechanism depend on the weight of the heatsink and the level of shock and vibration that the system must support. The overall structural design of the baseboard and system must be considered when designing the heatsink attachment mechanism. Their design should provide a means for protecting socket solder joints, as well as preventing package pullout from the socket.

Please note that the load applied by the attachment mechanism must comply with the processor mechanical specifications, along with the dynamic load added by the mechanical shock and vibration requirements, as discussed in Package Loading Specifications on page 42.

A potential mechanical solution for heavy heatsinks is the use of a supporting mechanism such as a backer plate or the utilization of a direct attachment of the heatsink to the chassis pan. In these cases, the strength of the supporting component can be utilized rather than solely relying on the baseboard strength. In addition to the general guidelines given above, contact with the baseboard surfaces should be minimized during installation in order to avoid any damage to the baseboard.

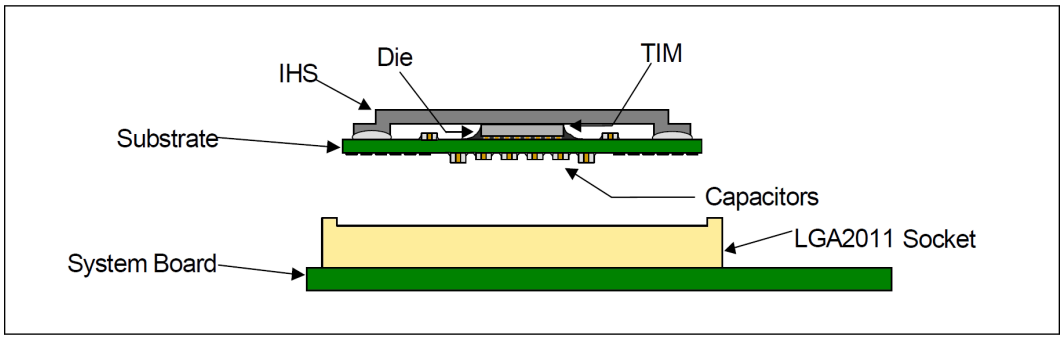
6.0 Processor Mechanical Specifications

The processor is packaged in a Flip-Chip Land Grid Array (FCLGA10) package that interfaces with the baseboard via an LGA2011-3 socket. The package consists of a processor mounted on a substrate land-carrier. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the mating surface for processor component thermal solutions, such as a heatsink. Diagram below shows a sketch of the processor package components and how they are assembled together.

The package components shown below include the following:

1. Integrated Heat Spreader (IHS)
2. Thermal Interface Material (TIM)
3. Processor core (die)
4. Package substrate
5. Capacitors

Figure 21. Processor Package Assembly Sketch



Notes:

- Socket and baseboard are included for reference and are not part of processor package.
- Processor package land count may be greater than socket contact count

6.1 Package Loading Specifications

The following table provides load specifications for the processor package. These maximum limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Exceeding these limits during test may result in component failure. The processor substrate should not be used as a mechanical reference or load bearing surface for thermal solutions.

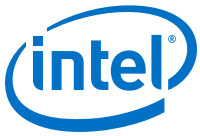


Table 15. Processor Loading Specifications

Parameter	Maximum	Notes
Static Compressive Load	1068 N (240 lbf)	This is the maximum static force that can be applied by the heatsink and Independent Loading Mechanism (ILM).
Dynamic Load	540 N (121 lbf)	Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement. This load will be a function of the geometry and mass of the enabling components used.
Notes: • These specifications apply to uniform compressive loading in a direction normal to the processor IHS. • See Socket Loading Specifications on page 16 for minimum socket load to engage processor within socket.		

6.2 Processor Mass Specification

The typical mass of the processor is currently 45 grams. This mass [weight] includes all the components that are included in the package.

6.3 Processor Materials

The table below lists some of the package components and associated materials.

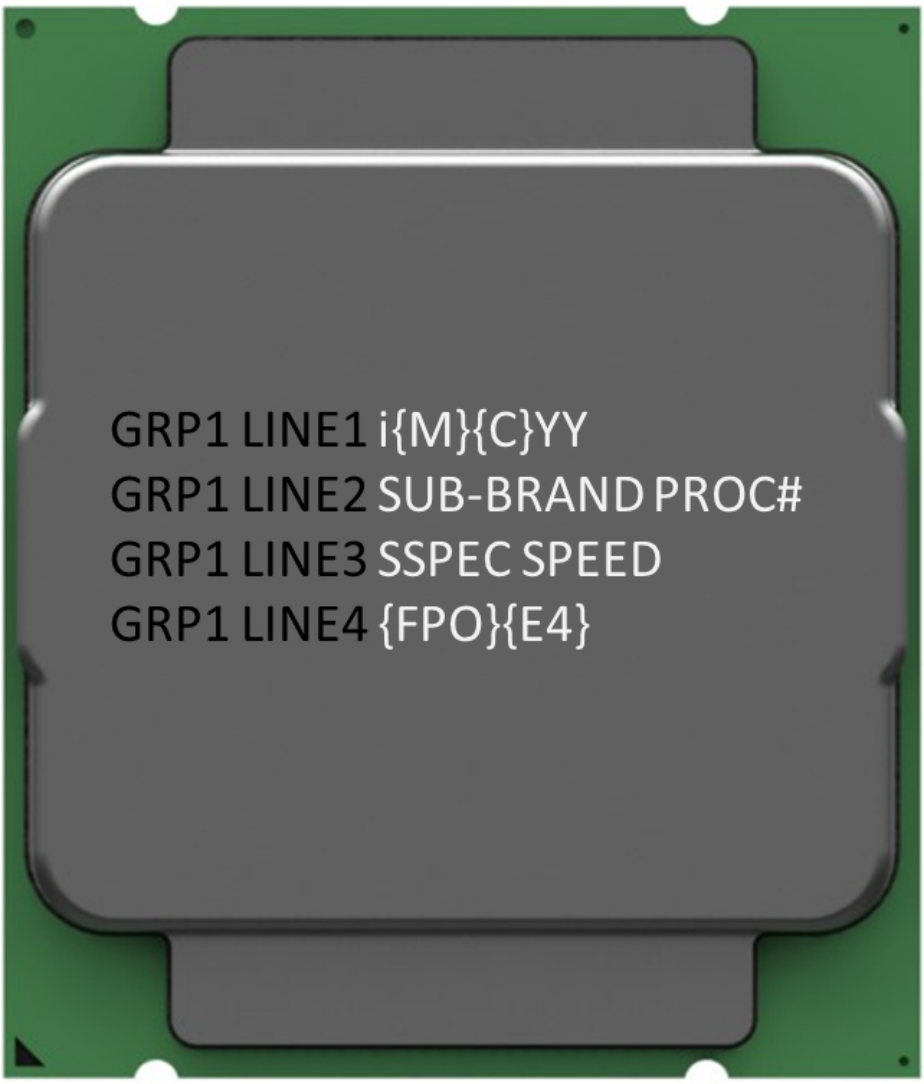
Table 16. Processor Materials

Component	Material
Integrated heat Spreader	Nickel Plated Copper
Substrate	Halogen Free, Fiber Reinforced Resin
Substrate lands	Gold Plated Copper

6.4 Processor Markings

Labeling locations and information are shown for the processor package in the following diagram.

Figure 22. Package Labeling



6.5 Package Handling Guidelines

The processor can be inserted into and removed from a socket 15 times. The following table includes a list of guidelines on package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

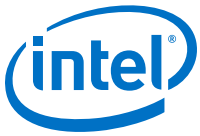


Table 17. Load Limits for Package Handling

Parameter	Maximum Recommended
Shear	356 N (80 lbf)
Tensile	156 N (35 lbf)
Torque	3.6 N-m (31.5 in-lbf)

7.0 Quality Reliability and Ecological Requirements

7.1 Use Conditions

Intel evaluates reliability performance based on the use conditions (operating environment) of the end product by using acceleration models.

The use condition environment definitions provided in the tables below are based on speculative use condition assumptions, and are provided as examples only.

Based on the system enabling boundary condition, the solder ball temperature can vary and needs to be comprehended for reliability assessment.

Use Environment	Speculative Stress Condition	Example Use Condition	Example 7 yr. Stress Equivalent	Example 10 yr. Stress Equivalent
Slow small internal gradient changes due to external ambient (temperature cycle or externally heated) Fast, large gradient on/off to max operating temp. (power cycle or internally heated including power save features)	Temperature Cycle	D T = 35 - 44°C (solder joint)	550-930 cycles Temp Cycle (-25°C to 100°C)	780-1345 cycles Temp Cycle (-25°C to 100°C)
High ambient moisture during low-power state (operating voltage)	THB/HAST	T = 25 -30°C 85%RH (ambient)	110-220 hrs at 110°C 85%RH	145-240 hrs at 110°C 85%RH
High Operating temperature and short duration high temperature exposures	Bake	T = 95 - 105°C (contact)	700 - 2500 hrs at 125°C	800 - 3300 hrs at 125°C

Use Environment	Speculative Stress Condition		Example Use Condition
Shipping and Handling	Mechanical Shock • System-level • Unpackaged • Trapezoidal • 25 g • velocity change is based on packaged weight		Total of 12 drops per system: • 2 drops per axis • ± direction
	Product Weight (lbs) < 20 lbs 20 to > 40 40 to > 80 80 to < 100 100 to < 120 ≥120	Non-palletized Product Velocity Change (in/sec) 250 225 205 175 145 125	
	Change in velocity is based upon a 0.5 coefficient of restitution.		
Shipping and	Random Vibration • System Level	Total per system: • 10 minutes per axis	

continued...

Use Environment	Speculative Stress Condition		Example Use Condition
Handling	• Unpackaged • 5 Hz to 500 Hz • 2.20 g RMS random • 5 Hz @ 0.001 g^2/Hz to 20 Hz @ 0.01 g^2/Hz (slope up) • 20 Hz to 500 Hz @ 0.01 g^2/Hz (flat) • Random control limit tolerance is ± 3 dB	• 3 axes	

7.2 Intel Reference Component Validation

Intel tests reference components individually and as an assembly on mechanical test boards and assesses performance to the envelopes specified in previous sections by varying boundary conditions.

While component validation shows a reference design is tenable for a limited range of conditions, customers need to assess their specific boundary conditions and perform reliability testing based on their use conditions.

Intel reference components are also used in board functional tests to assess performance for specific conditions.

7.2.1 Board Functional Test Sequence

Each test sequence should start with components (baseboard, heatsink assembly, and so on) that have not previously endured any reliability testing.

Prior to the mechanical shock and vibration test, the units under test should be preconditioned for 72 hours at 45°C. The purpose is to account for load relaxation during burn-in stage.

The test sequence should always start with a visual inspection after assembly, and BIOS/processor/memory test. The stress test should be then followed by a visual inspection and then BIOS/processor/memory test.

7.2.2 Post-Test Pass Criteria Examples

The post-test pass criteria examples are:

1. No significant physical damage to the heatsink and retention hardware.
2. Heatsink remains seated and its bottom remains mated flat against the IHS surface. No visible gap between the heatsink base and processor IHS. No visible tilt of the heatsink with respect to the retention hardware.
3. No signs of physical damage on baseboard surface due to impact of heatsink.
4. No visible physical damage to the processor package.
5. Successful BIOS/Processor/memory test of post-test samples.
6. Thermal compliance testing to demonstrate that the case temperature specification can be met.

7.2.3 Recommended BIOS/Processor/Memory Test Procedures

This test is to ensure proper operation of the product before and after environmental stresses, with the thermal mechanical enabling components assembled. The test shall be conducted on a fully operational baseboard that has not been exposed to any battery of tests prior to the test being considered.

Testing setup should include the following components, properly assembled and/or connected:

- Appropriate system baseboard.
- Processor and memory.
- All enabling components, including socket and thermal solution parts.

The pass criterion is that the system under test shall successfully complete the checking of BIOS, basic processor functions and memory, without any errors. Intel PC Diags is an example of software that can be utilized for this test.

7.3 Material and Recycling Requirements

Material shall be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal and vegetable based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (for example, polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance. Cadmium shall not be used in the painting or plating of the socket. CFCs and HFCs shall not be used in manufacturing the socket.

Any plastic component exceeding 25 gm should be recyclable per the European Blue Angel recycling standards.

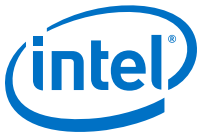
Supplier is responsible for complying with industry standards regarding environmental care as well as with the specific standards required per supplier's region. More specifically, supplier is responsible for compliance with the European regulations related to restrictions on the use of Lead and Bromine containing flame-retardants. Legislation varies by geography, European Union (RoHS/WEEE), China, California, and so forth.

The following definitions apply to the use of the terms lead-free, Pb-free, and RoHS compliant.

Halogen flame retardant free (HFR-Free) PCB: Current guidance for the socket pad layout supports FR4 and HFR-Free designs. In future revisions of this document, Intel will be providing guidance on the mechanical impact to using a HFR-free laminate in the PCB. This will be limited to workstations.

Lead-free and Pb-free: Lead has not been intentionally added, but lead may still exist as an impurity below 1000 ppm.

RoHS compliant: Lead and other materials banned in RoHS Directive are either (1) below all applicable substance thresholds as proposed by the EU or (2) an approved/ pending exemption applies.



Note: RoHS implementation details are not fully defined and may change.

Appendix A Component Suppliers

Customers can purchase the Intel reference or collaboration thermal solutions from the suppliers listed in the following table.

Table 18. Intel® Reference or Collaboration Thermal Solutions

Item	Intel Part Number	Supplier PN	Delta Supplier Contact Info	Foxconn Supplier Contact Info
Thermal Interface Material (TIM)	N/A	PCM45F	Honeywell	Judy Oles judy.oles@honeywell.com +1-509-252-8605
		TC-5022	Dow Corning	Ed Benson e.benson@dowcorning.com +1-617-803-6174
Liquid Cooling Solution (TS13X)	G31573-001	TS13X	Intel	

Customers can purchase the Intel LGA2011-3 sockets and reference LGA2011-3 ILMs from the suppliers listed in the following table.

Table 19. LGA2011-3 Socket and ILM Components

Item	Intel PN	Foxconn (Hon Hai)	Tyco	Lotes	Amtek	Molex
LGA 2011-3 Socket POR	G64443-001	PE201127-4355-01H	2201838-1	NA	NA	NA
LGA 2011-3 Square ILM	G63449-005	PT44L11-4711	2229339-2	AZIF0018-P001C	ITLG63449001	105274-2000
LGA 2011-3 Backplate	E91834-001	PT44P41-4401	2134440-1	DCA-HSK-182-T02	ITLE91834001	105142-7000
Supplier Contact Info		Eric Ling eric.ling@foxconn.com 503-693-3509 x225	Alex Yeh alex.yeh@te.com Tel: +886-2-21715280	Cathy Yang Cathy@lotes.com.cn Tel: +1-86-20-84686519	Alvin Yap alvinyap@amtek.com.cn Tel +(86)752-2634562 Cathy Yu cathy_yu@amtek.com.cn Tel +(86)752-2616809	Edmund Poh edmund.poh@molex.com Tel +1-630-718-5416

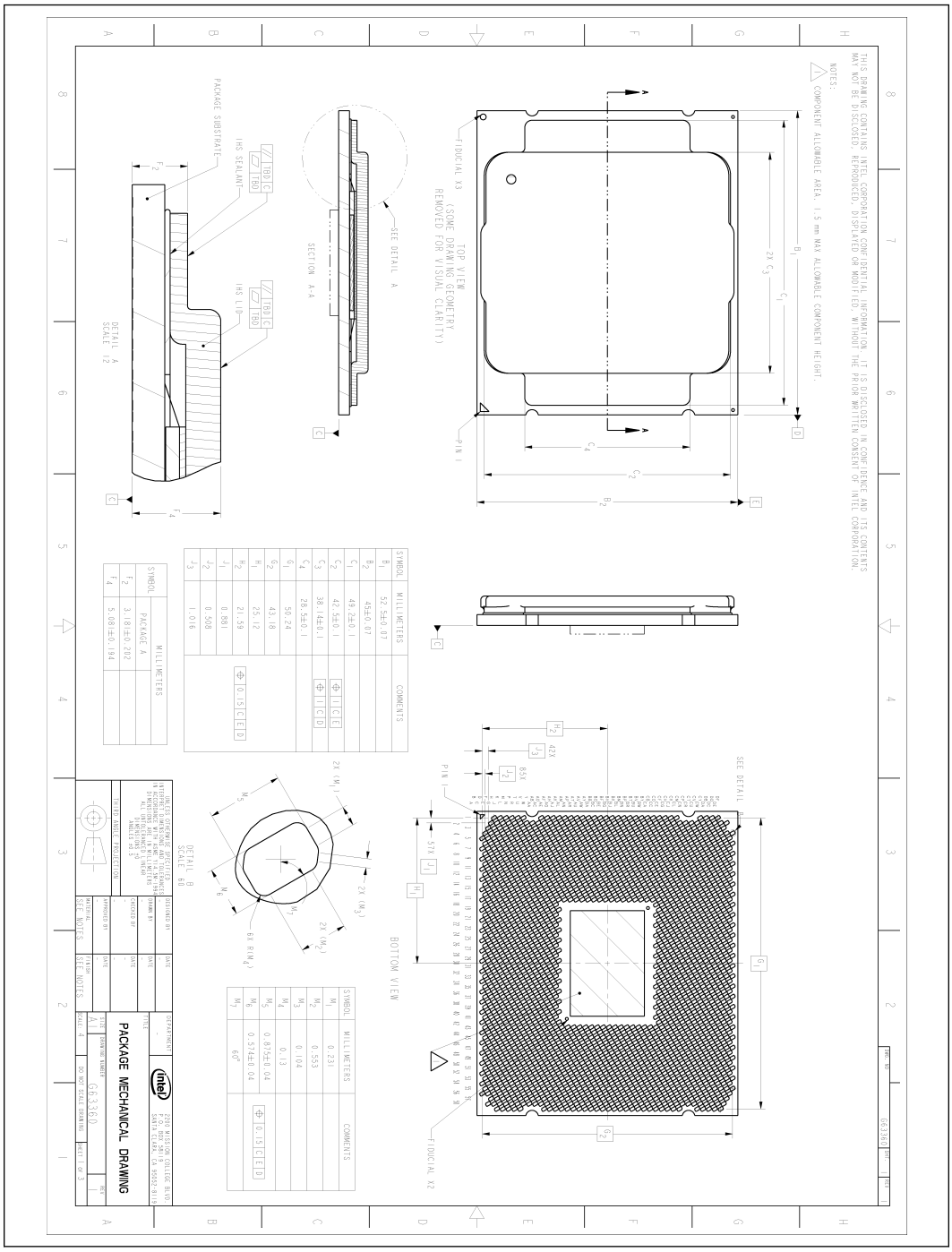
Appendix B Mechanical Drawings

The following sections contain mechanical drawings of reference retention designs, processor package geometry and reference heatsink designs.

Table 20. List of Mechanical Drawings

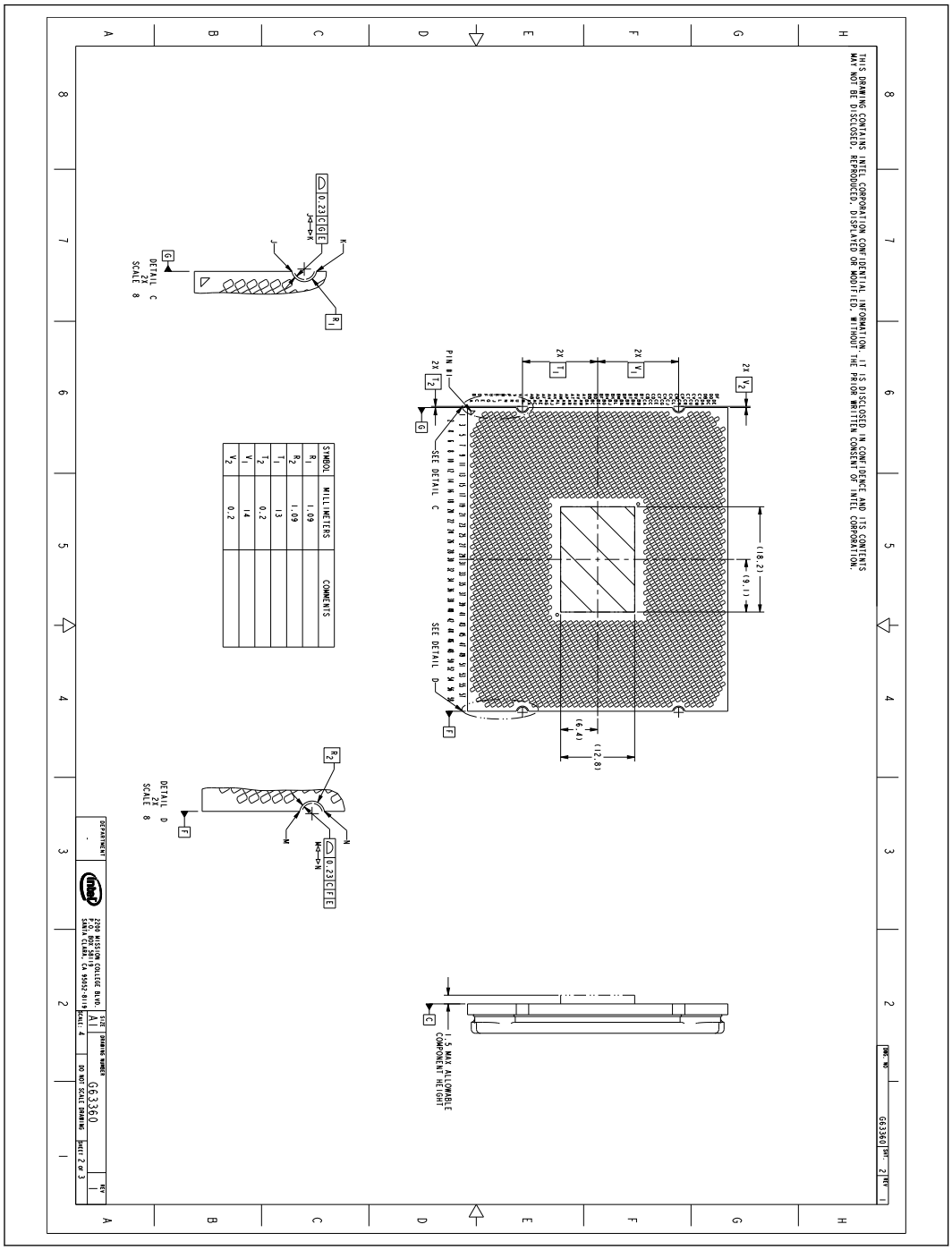
B.1 Package Mechanical Drawing Page 1

Figure 23. Package Mechanical Drawing Page 1



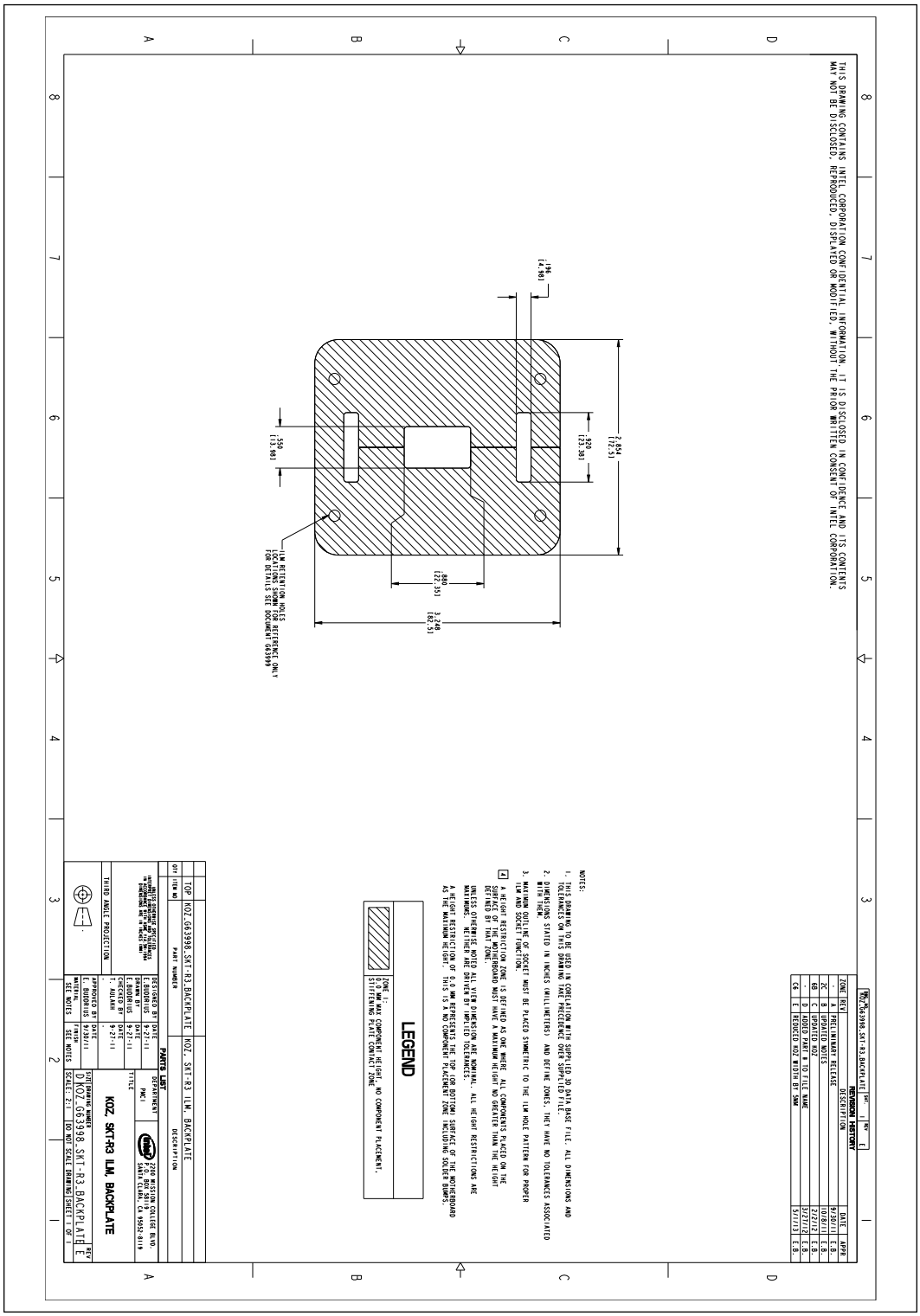
B.2 Package Mechanical Drawing Page 2

Figure 24. Package Mechanical Drawing Page 2



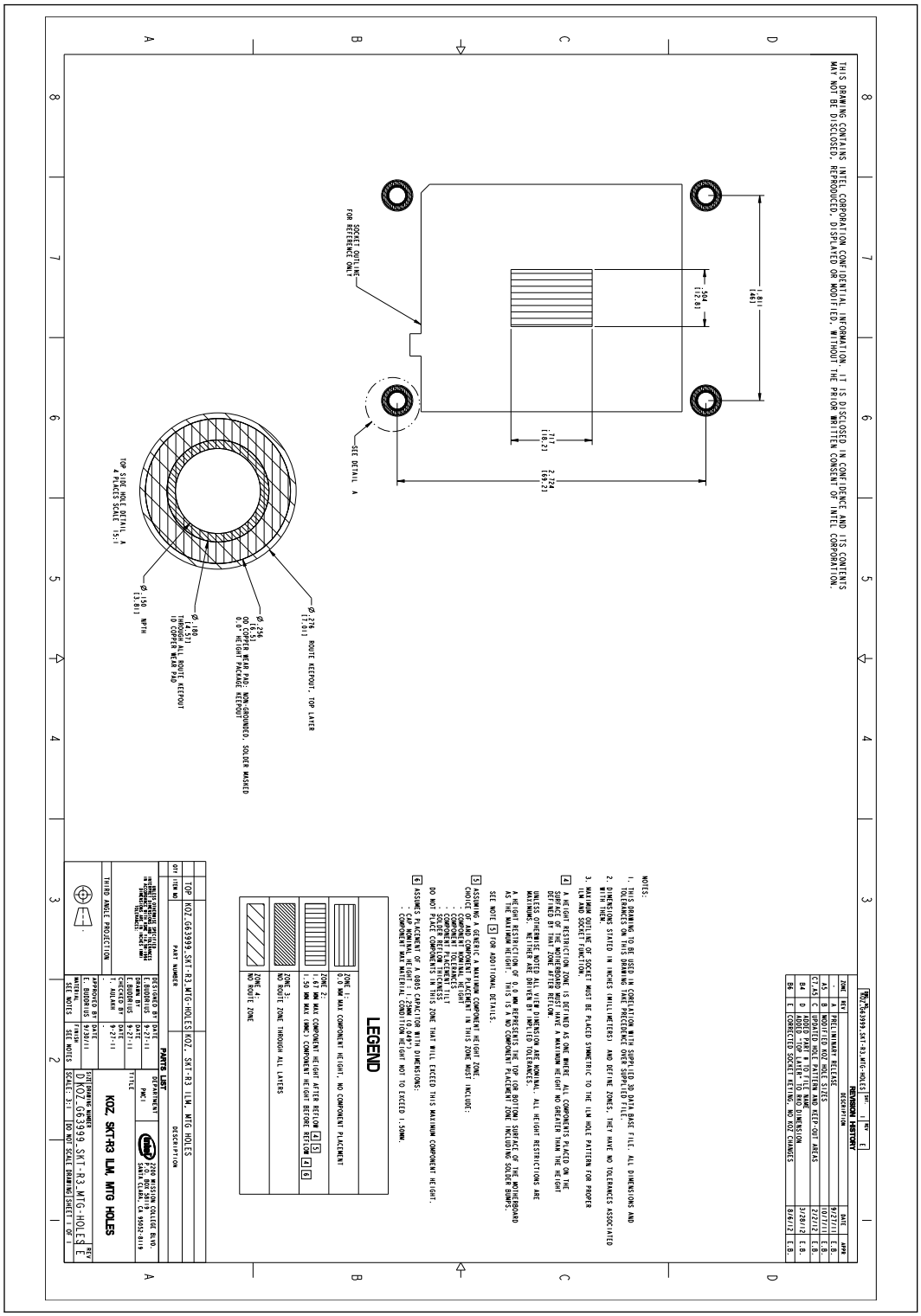
B.3 ILM Backplate Keep Out Zone

Figure 25. ILM Backplate Keep Out Zone



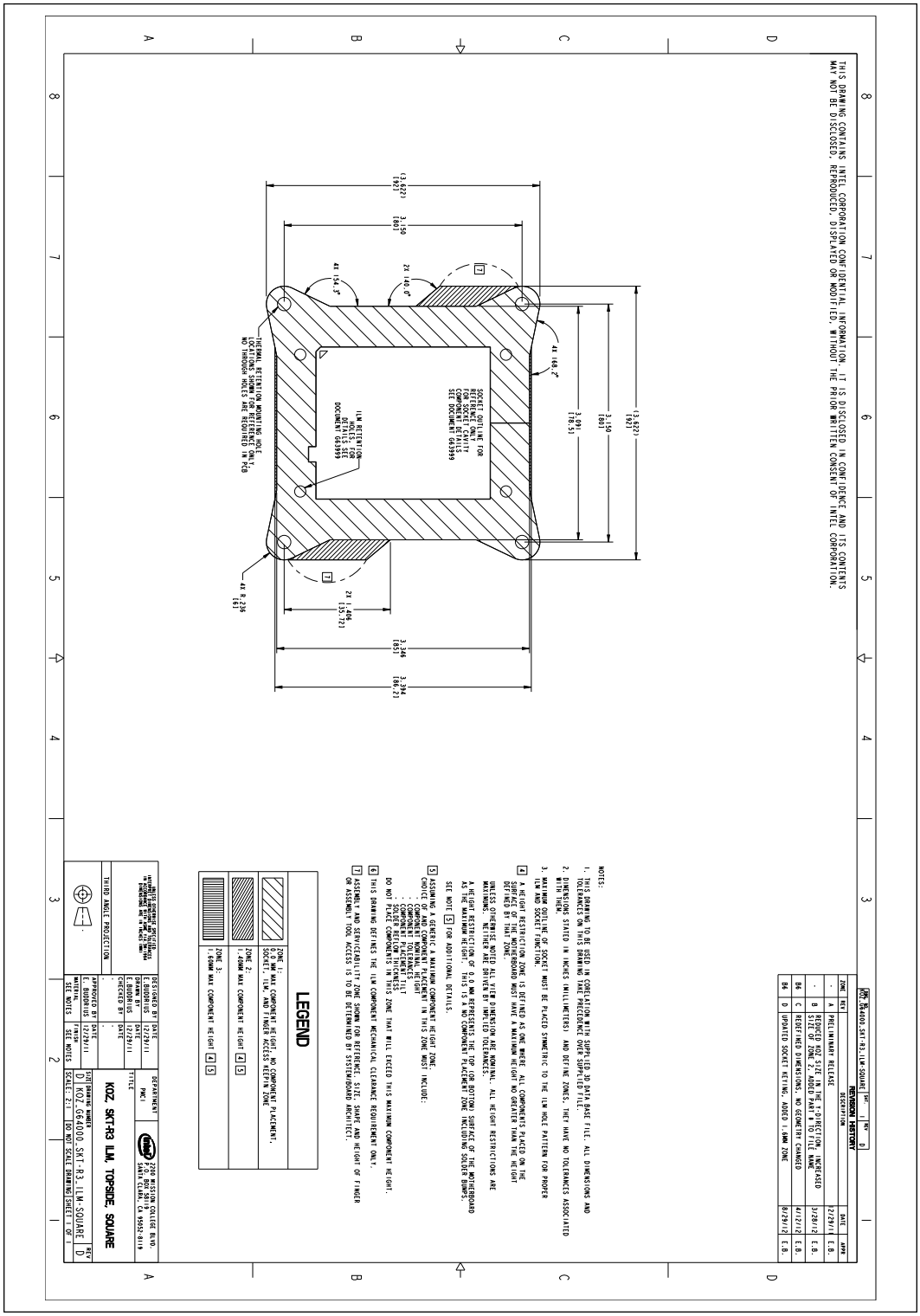
B.4 ILM Mounting Hole Keep Out Zone

Figure 26. ILM Mounting Hole Keep Out Zone



B.5 ILM Keep Out Zone

Figure 27. ILM Keep Out Zone



B.6 3D Keep Out Zone

Figure 28. 3D Keep Out Zone